EFFECTIVE PLANAR METHOD OF DEFECTS GETTERING

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It was shown that treatment of polycrystalline silicon films of small grain size in a atmosphere of oxygen leads to a decrease in their resistance owing to recrystallization of the grains, whereas during the annealing of films of large grain size the oxidation of intergrain boundaries is the dominant process resulting in an increase in the resistance.

The planar arrangement of gettering centers at close distance to active elements make process of gettering independent of duration and temperature technological processes and therefore increase their effectiveness without additional technological operation of the insertion of the gettering centers.

1. Introduction

Polycrystalline silicon (poly-Si) films are frequently used in semiconductor devices and integrated circuit (IC) elements. In particular, p-n-junctions prepared by the local deposition of poly-Si films of one conductivity type onto monocrystalline silicon (mono-Si) substrates of the opposite conductivity type have been described in [1, 2], as well as resistors for monolithic ICs [3] based on deposited poly-Si films.

The characteristics of poly-Si and mono-Si films formed simultaneously during a single process of epitaxial growth on locally oxidized silicon substrates have been reported in [4]. Similar films may be used as discrete elements of ICs, their properties being determined by the requirements of the mono-Si films which depend on the class of the circuits in which the film is used.

The constant temperature of the industrial chloride process of epitaxy as well as the homogeneous surface of the amorphous SiO_2 films which seem to be a template for the growth of the local poly-Si films do not make it possible to control the parameters of the poly-Si films to be grown. It is well known that the basic parameters which determine the electrical properties of poly-Si films are mean grain size (determined by the temperature), the film thickness and the dopant concentration which are constant for a given class of circuit. Hence the films were grown on predeposited thin films of silicon which act as nucleation layers.

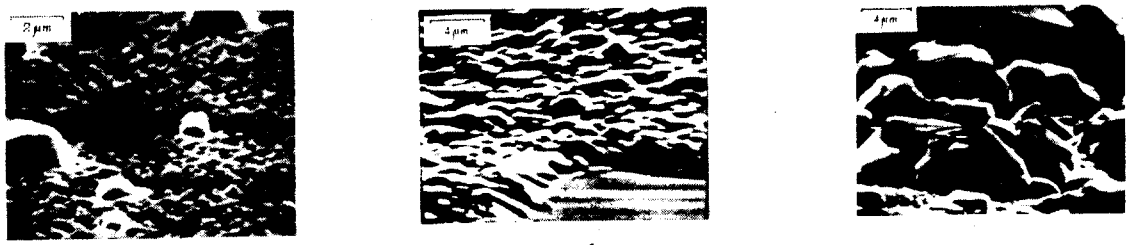
The main aim of this study was to investigate the structure and electrical properties of poly-Si films grown on the nucleation layers at various deposition temperatures.

2. Sample preparation

The samples were fabricated on silicon substrate of p-type conductivity, orientation (111) and resistivity 10 Ω·cm. The substrates were oxidized to obtain a thermal oxide layer of 0.5 μm thick onto which a thin undoped nucleation layer of about 100Å thick was deposited by the low temperature process of monosilane pyrolysis (800-860°C). Using photolithography and etching we obtained the local nucleation areas onto them. Then a vertical reactor heated by high frequency power was used for the epitaxial growth of the n-type film by a high temperature chloride process (1220°C) carried out according to the technology described in [5]. The films were doped by phosphorus with the addition of phosphine to the float at a partial pressure of 6.8 Torr. The thickness of the films was 5 μm, and the dopant concentration was $10^{16}cm^{-3}$, as determined by the four-probe method on the monocrystalline substrate.

3. Experimental data

When the films were studied by scanning electron microscopy it was found that an increase in the deposition temperature of the nucleation layer from 800° to 860°C results in an increase in the grain size by a factor of 10 (fig. 1). The poly-Si films grown on a nucleation layer deposited at 800°C were fine grained, the size of the spherical grains being not more than 0.5 μm. However, the films contained rather large edge blocks 2-3 μm in size (fig. 1,a). The films grown on a nucleation layer deposited at 830°C had the most uniform structure with a grain size of 1-2 μm (fig. 1,b), while for a high deposition temperature of the nucleation layer (860°C) the poly-Si films had a grain size of 4-5 μm and their structure was non-uniform showing occasional formations and monoblocks up to 10 μm (fig. 1,c).



a b c

Fig. 1. The structure of poly-Si films grown on nucleation layers deposited at various temperatures: (a) 800°C; (b) 830°C; (c) 860°C

The results show that in spite of the higher film growth temperature in the chloride process the size of the grains is determined by the deposition temperature of the nucleation layer.

The electrical resistance of poly-Si films of size 200μm×20μm grown on nucleation layers deposited at different temperatures were determined from measurements of the voltage divided by the current. There was a considerable spread in the resistances of the films. It should be noted that at low applied voltages (up to 1 V) an increase in the temperature deposition of the nucleation layer results in a decrease in the resistance by a factor 10 (fig. 2,a). When the applied voltage exceeded 1V, the resistance of the fine-grained films decreased markedly, becoming lower than that of the film grown on the nucleation layer deposited at 830°C. The films grown on the nucleation layers whose deposition temperatures were 830° and 860°C showed slight changes in resistance when the voltage was increased. The films with a coarse-grained structure had the lowest resistance over the entire range of voltage.

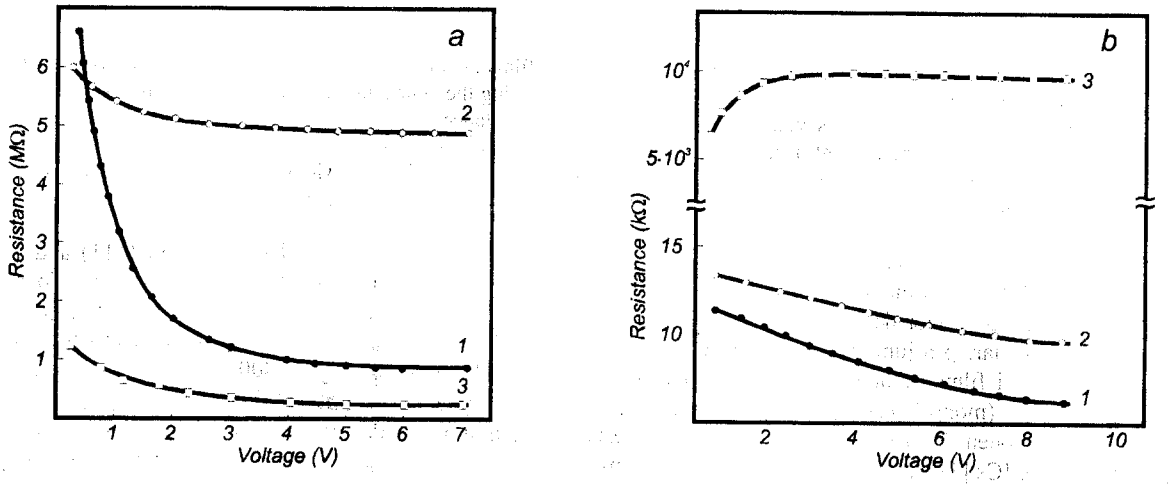


Fig. 2. Voltage-resistance characteristics of poly-Si films of different structures (a) before the heat treatment and (b) after the heat treatment: curves 1, 800° C; curves 2, 830° C; curves 3, 860° C

Since the simultaneous growth of the poly-Si and mono-Si films on a single substrate offers good possibilities for their use as IC elements, it seemed to be appropriate to study the effect of heat treatment, which conforms to the technology of the manufacture of the active elements, on the electrical characteristics of the poly-Si films. For this purpose the samples were subjected to consecutive heat treatments at a temperature of 1000°C (oxidation; 45 min) in wet oxygen, at a temperature of 1150°C (base formation; 1.5 h) in a mixture of oxygen and nitrogen and at a temperature of 1050°C (emitter formation; 50 min) in oxygen, the total time being over 3 h.

After heat treatment the size of the grains in the fine-grained samples had increased with the result that the electrical resistance of the films had decreased (fig. 2,b). The resistance of the coarse-grained films (860°C) had increased to 50-100 MΩ.

For the coarse-grained film structure consisting of two monocrystalline areas separated by a poly-Si film with an area of 10^{-5}cm^2 the breakdown voltages were 50-60 V after a complete heat treatment, the leakage current density being 10^{-2}A·mm^{-2}. This demonstrates the possibility of utilizing these films as an insulating material for IC elements.

4. Application

Increasing reliability VLSI in certain extent depends of substrate enhancement, reduction of damage and p-n-junction leakage. It is known, that bipolar transistors with narrow base are very sensitive to existence of precipitates of metallic impurity, which display itself as generation-recombination centers and circuit regions of emitter with collector [6].

There are methods of gettering which are based on previously introducing of damage into back side of substrate. This damage captures and holds impurity in during the high temperature technological operation. For this purpose additional operation is used, for example, mechanical thermal or laser treatment [7].

The problem is that gettering centers are located on the back side of substrate and during implementation of technological operations metallic impurities have to be diffused across substrate thickness, which is approximately 450 μm. However, recently there is a tendency towards reduction of temperature and duration of processing. At the same time the diffusivity of impurities atoms sharply decreases and the duration of the operation can be not sufficient for the atoms to reach the gettering centers on the rewards side substrate.

A technology of simultaneous growth of mono- and polycrystalline silicon films in the single epitaxial processing makes it possible to form local regions of the poly-Si films required configuration, which act themselves as gettering centers.

The density surface states N_{SS} are the most sensitive characteristic to the defects of devices. Therefore we fabricated the test MOS-structure, the C-V-characteristics of which was investigated. The capacitance-voltage characteristics were measured with an L2-7 impedance bridge at room temperature over frequency range 0.465-10 MHz, using an ac signal of low voltage (25 mV).

Calculation of interface Si-SiO_2 charge was done by formula

$$\left(Q_{ox} + Q_{SS}\right)^{FB} = \Delta U_g^{FB} C_o \,, \qquad (1)$$

where C_o is undergate oxide capacity; ΔU_g^{FB} is a shift of experimental curve about theoretical in the point of flat band capacity C_S^{FB}.

$$C_S^{Fb} = g\left(\varepsilon_S N_D / kT\right)^{1/2}. \quad (2)$$

For determination of surface states charge Q_{SS} required to find capacity of semiconductor in the point of inversion

$$C_S^{inv} = \left[q\varepsilon_S N_D / 2\left(U_g^{inv} - \varphi_S\right)\right]^{1/2}. \quad (3)$$

Then by the help of the formula (1) the calculate full charge interface $Si-SiO_2$ in the point of inversion and substract from full charge in the point of flat band. The calculation showed, that N_{SS} on the samples, around polysilicon films, two order less, than in the samples, around p-n-junction isolated.

The planar arrangements of gettering centers at close distance to active elements IC makes the process of gettering independent from duration and temperature technological processes and therefore increase their effectiveness without additional operation of the insertion of the gettering centers.

[1] *Zvy and B.-L.Adiz.* IEEE Trans. Electron Devices, 1977, №24, p.1025.

[2] *L.D.Lopatina, V.L.Sukhanov and V.V.Tuchkevich.* Pisma Zh. Eksp. Teor. Fiz., 1979, №5, p.11.

[3] *F.D.King and G.Shewchun.* Solid-State Electron., 1973, №16, p.701.

[4] *M.A.Garibov, F.D.Kasimov and V.M.Mamikonova.* Izv. Akad. Nauk AzSSR., Ser. Fiz-Tekh. Mat. Nauk, 1979, №4, p.91.

[5] *F.D. Kasimov and B.Kh. Mamedov.* Electron. Tekh., Ser. Materiali., 1984, №5, p.23.

[6] *C.W. Pearce, L.E. Katz and T.E. Seidel.* Considerations regarding gettering in integrated circuits., Electrochem. Soc., Pennington New Jersey, 1981.

[7] *B. Hartiti and J. Muller.* IEEE Trans. Electron. Devices, 1992, №39, p.27.

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DEFEKTLƏRİN PLANAR HETTERİRLƏNMƏSİNİN EFFEKTİV METODU

Göstərilmişdir ki, kiçik dənəcikli polikristallik silisium təbəqələrinin (PST) oksigen mühitində termik işlənməsi dənəciklərin rekristallizasiya sayəsində onların elektrik müqavimətinin azalmasına gətirib çıxarır, baxmayaraq ki, iri dənəcikli təbəqələrdə dənəciklər sərhəddinin oksidləşməsi prosesi üstünlük təşkil edir, bu da ki muqaviməti artırır.

PST-də hetterirləmə mərkəzlərinin planar yerləşməsi aktiv elementlərin yaxın məsafələrində hetterirləmə proseslərinin zamandan və texnoloji proseslərin temperaturundan qeyri asılı edir və əlavə əməliyyatlar aparmadan onun effektivliyini artirir.

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ЭФФЕКТИВНЫЙ МЕТОД ПЛАНАРНОГО ГЕТТЕРИРОВАНИЯ ДЕФЕКТОВ

Показано, что термообработка мелкозернистых пленок поликристаллического кремния (ППК) в атмосфере кислорода ведет к уменьшению их электрического сопротивления благодаря рекристаллизации зерен, в то время как в крупнозернистых пленках доминирующим процессом является прокисление границ зерен, что приводит к увеличению сопротивления.

Планарное расположение геттерирующих центров, каковыми являются ППК, на близких расстояниях от активных элементов делает процесс геттерирования независимым от времени и температуры технологических процессов и увеличивает его эффективность без проведения дополнительных операций.

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