CURRENT-CONDUCTION MECHANISM IN Al/p-Si SCHOTTKY BARRIER DIODES (SBDs) WITH NATIVE INSULATOR LAYER

ŞEMSETTİN ALTINDAL, HAVVA KUTLUCA
Physics Department,
Faculty of Arts and Sciences,
Gazi University, Ankara, Turkey

TOFIG MAMMADOV, MEHMAN ŞİRİNOV
National Academy of Science,
Institute of Physics,
Azerbaijan, AZ-1143, Baku, G.Javid ave., 33

В температурном интервале 295-400K исследованы вольтамперные (*I-V*) характеристики SDs. Анализ переднего наклона I-*V* характеристик, основанный на механизме термоэлектронной эмиссии (ТЭ) выявил уменьшение фактора идеальности (*n*) и увеличение нулевого наклона высоты барьера (Φ_{Bo}) с увеличением температуры. Изменения величин (*n*) и (Φ_{Bo}) от 1.76 до 1.48 и от 0.756 до 0.880eV показывают, что в Al/SiO_2/p-Si диоде не соблюдается чистый (ТЭ) механизм. Поэтому, мы предлагаем модификацию, включающую n и параметр туннелирования $\alpha\chi^{0.5}\delta$ в выражении обратного тока насыщения I_o. Измерения полулогарифмического переднего наклона LnI-*V* указывает на механизм токовой проводимости нашего образца в области промежуточного наклона и температурной области 295-400K, который был исследован в этой работе, как доминирующее многошаговое туннелирование через ловушки.

The current-voltage (*I-V*) characteristics of SDs in the temperature range of 295-400 K are investigated. The analysis of the experimental forward bias I-*V* characteristics based on the thermionic emission (TE) mechanism has revealed a decrease of the ideality factor (*n*) and increase of the zero-bias barrier height (Φ_{Bo}) with the increase of temperature. The *n* and Φ_{Bo} values change from 1.76 to 1.48 and 0.756 to 0.880eV are indicating that the Al/SiO_2/p-Si diode does not obey the pure TE mechanism. Therefore, we have reported a modification which is includes the n and tunneling parameter $\alpha\chi^{0.5}\delta$ in the expression of reverse saturation current Io. The semi-logarithmic forward bias LnI-*V* measurements suggested that predominant current conduction mechanism of our sample in the intermediate bias region and temperature region of 295-400 K investigated in this work was dominated by a trap-assisted multistep tunneling.

INTRODUCTION

Because of the technical importance of the Schottky barrier at metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) Schottky diodes, they have been thoroughly investigated [1-6] for a long time. However, the current transport mechanisms in these structures are not fully understood yet. There are several reasons, which cause the device to deviate from the ideal behavior, and must be taken into account. These include the effects of interfacial insulator layer, interface states and carrier transport mechanism. In order to find whether the fabricated Schottky diode (SD) is ideal or not, the forward bias *J-V* and reverse bias *C-V* characteristics at a temperature range are considered. The presence of the interfacial insulator layer and interface states strongly influence the electrical characteristics of a MIS device. Schottky barrier height (SBH) and ideality factor are the fundamental parameters of the MIS diodes and these parameters have strong effect on devices performance. Understanding the current-conduction mechanism in metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) SDs on a fundamental basis still remains a challenging problem. It has been well known that there are currently a vast number of reports on experimental studies of SDs in a great variety of MS, MIS structures and solar cells [1-17]. They are important research tools in both constructing some useful devices in technology and studying semiconductor surface. There is several possible sources error, which cause deviation from the ideal behavior, and must be taken into account. In generally, these include the effects of interfacial insulator layer, interface states and series resistance. A number of carrier-conduction mechanism such as thermionic emission (TE), thermionic field emission (TFE), minority carrier injection, recombination-generation and multistep tunnelling compete, and one of them usually may dominate over the others in certain temperature and voltage region[1,2]. However simultaneous contribution from two or more mechanism could also be possible. In this study, temperature dependent *I-V* characteristics of Al/SiO_2/p-Si Schottky diodes with interfacial insulator (SiO_2) layer are reported in the temperature range 295-400 K. Experimental results show that the forward current transport is predominantly characterized by a trap-assisted multistep tunnelling mechanism at all temperature.

EXPERIMENTAL DETAILS

The Al/SiO_2/p-Si Schottky diodes were fabricated on a quarter of 2 inch diameter float zone <100> p-type B (boron) doped single crystal silicon wafer having thickness of 350 μm with ~1 Ω-cm resistivity. For the fabrication process, Si wafer was decreased in organic solvent of $CHCLCCL_2$, CH_3COOH_3 and CH_3OH, etched in a sequence of H_2SO_4 and H_2O_2, 20 % HF, a solution of 6 HNO_3: 1HF:35H_2O, 20 % HF and finally quenched in de-ionized water with resistivity of 18 MΩ-cm for 3 minutes. The Al back contact (with a thickness of 2000 Å and % 99.999 impurity) was thermally evaporated by means of a tungsten filament onto the whole back side of in quarter Si wafer under a pressure of ~$2x10^{-6}$ Torr in an oil vacuum pump system. The ohmic contact was formed by sintering the evaporated Al back contact at 600 ^oC for 60 minutes in flowing dry nitrogen (N_2) ambient at a rate of 2 liter/min. This process served both to sinter the Al and to form the required thin insulator layer (SiO_2) on the upper surface of the Si wafer. After the thermal treatment Al circular dots having area of about 0.02 cm^2 and 2500 Å thick aluminum rectifying contacts were deposited at a rate of about 4 Å/s onto the SiO_2 surface of the wafer through a metal shadow mask in liquid nitrogen trapped oil-free vacuum system in the pressure of $2x10^{-6}$ Torr. The metal layer thickness and the deposition rates were monitored with the help of quartz crystal thickness monitor. The interfacial oxide layer thickness was estimated from the measurement of the oxide capacitance in the strong accumulation region according ref.[9]. The temperature dependence of current density-voltage-temperature (J–*V*-*T*) measurements was performed by the use of a Keithley 220 programmable constant current source together with a Keithley 614 electrometer. All measurements were carried out the same sample to avoid the effect of the film thickness and performed under (≤ 10^{-3} mbar) and in the dark.

RESULTS AND DISCUSSION

In order to determine the dominant current transport mechanism of the Al/SiO_2/p-Si (MIS) type Schottky diodes, we measured the forward bias *J-V* characteristics as a function of temperature. For a SBD with an interface oxide layer, it is assumed that the relationship between the applied forward bias ($V > 3\ kT/q$), and current density of the device is due to the TE theory and it can be written as [1-3]

$$J = J_o \exp\left(\frac{qV_d}{nkT}\right)\left[1 - \exp(-\frac{qV_d}{kT}\right] \quad (1)$$

where *n* is the ideality factor, *k* is the Boltzmann constant and *T* is the temperature in Kelvin. J_o is the reverse saturation current density and expressed as

$$J_o = A^* \ T^2 \exp(-q\Phi_{Bo} / kT) \quad (2)$$

where the quantities A^*, Φ_{Bo} are the effective Richardson constant and the zero-bias barrier height, respectively. Fig. 1 shows the temperature dependence of the forward bias Ln*J-V* characteristics of one of our samples (Al/SiO_2/p-Si Schottky diodes) in the temperature range of 295 K-400 K

The I_o was obtained by extrapolating the linear intermediate voltage region of the curve to zero-applied voltage and the Φ_{Bo} values were obtained at each temperature from Eq.(2) and given in Table 1. The insulator layer (SiO_2) thickness was obtained from sufficiently high frequency (500 kHz) *C-V* characteristics using the equation for insulator layer capacitance $C_i = \varepsilon_i\varepsilon_o A/\delta$, where $\varepsilon_i = 3.8\ \varepsilon_o$, ε_i and ε_o are the permittivities of the interfacial layer and free space, respectively [9]. As can be seen in Table 1, the Φ_{Bo} obtained from forward bias *I-V* characteristics shows an unusual behavior that it increases with the increase of temperature. Such behavior is an obvious disagreement with the reported negative temperature coefficient of barrier height or Si band-gap. In order to examination of the dependence of *n* on temperature we plotted *n*-1000/*T* and ıt found a linear plot over the whole temperature range. The change in *n* with temperature is seen in Table 1, and *n* can be represented by the following expression as

$$n(T) = n_o + T_o / T \quad (3)$$

where the n_o and T_o are constant which were found to be 0.285 and 788 K, respectively. The thermionic-field emission (TFE) mechanism can also be rule out in observed region, since *nT* is more or less constant in all temperature range. Using the $\alpha\chi^{0.5}\delta$ factor 12, T dependent (Φ_{Bef}) is obtained each T and is given in Table 1. Furthermore, T dependence Φ_{Bef} can be described as

$$\Phi_{Bef}(T) = \Phi_{Bef}(0\ K) + \alpha T \quad (4)$$

where α is t coefficient of BH. Fitting of Φ_{Bef} vs T yields Φ_{Bef}(0 K)=1.06 eV and $\alpha = -8.93x10^{-4}$ eV/K.

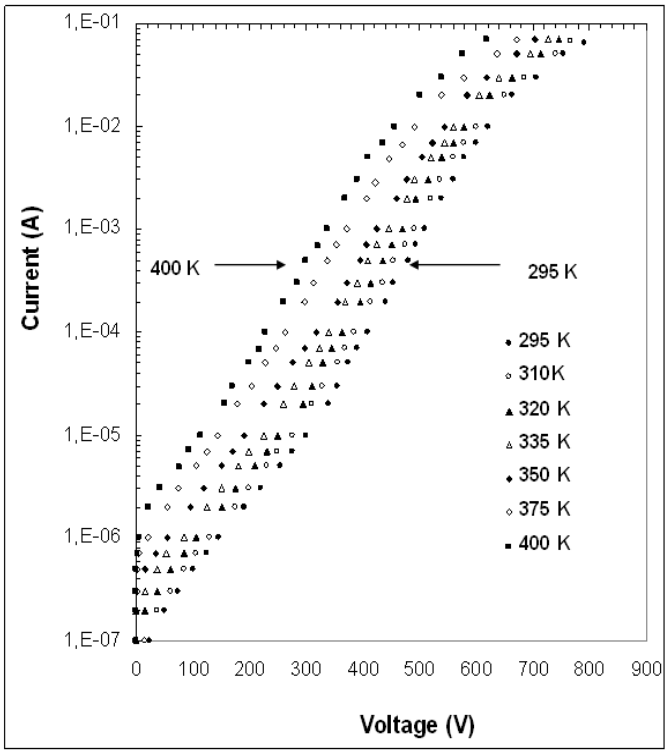

Fig. 1. Forward *I-V-T* characteristics of the Al/SiO_2/p-Si Schottky diode.

Experimental plots of *kT/q* against E_o in Fig. 2 indicate that TFE can not the process responsible for the current transport. The minority carrier diffusion is also unlikely for our sample, since it would be expected [7] to be significant only for devices having very high effective barrier height value near to the band gap of Si and very low reverse saturation current density with temperature independent diode ideality factor having value of almost unity.

Table 1

Temperature dependent values of various parameters determined from *I-V* measurements.

T (K)	n	Io (A)	Φ_{Bo} (eV)	Φ_{Bef} (eV)	Tanθ=q/(nkT) (eV^{-1})
295	1.76	$1.11x10^{-8}$	0.756	0.793	22.31
310	1.71	$2.19x10^{-8}$	0.779	0.783	21.92
320	1.65	$3.43x10^{-8}$	0.793	0.762	21.94
335	1.64	$8.00x10^{-8}$	0.808	0.756	21.15
350	1.62	$1.68x10^{-7}$	0.825	0.750	20.36
375	1.54	$4.65x10^{-7}$	0.855	0.745	20.06
400	1.48	$7.4x10^{-7}$	0.880	0.740	19.60

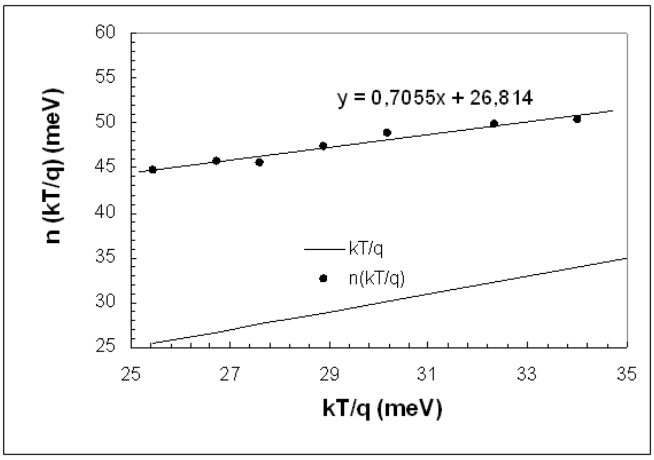

Fig. 2. Tunnelling current parameter E_o (nkT/q) - kT/q for Al/p-Si Schottky diode

Also the slope of the Ln *I* vs *V* plot (Table 1) is almost temperature independent and this behavior is quite suggestive of tunnelling conduction mechanism in the SDs dominating current flow through the junction. [7,18] the *I-V* relationship is given by [1,7,18].

$$I\,(V,T)=I_t \exp\,[A(V-V_d)] = J_o\,(T) \exp\,(AV) \quad (5)$$

where I_t is a constant proportional to the density to the density of traps of appropriate energy in the Si space charge region, V_d is the built-in or diffusion potential and A is a constant. We conclude that TE is not the limiting current transport mechanism in this voltage region. Therefore it seems that trap-assisted multistep tunnelling is the mechanism that dominates the forward bias *I-V* characteristics in this voltage and temperature range an all these result have suggest that the tunnelling plays an important role in the current transport [7,18,19].

CONCLUSION

The forward bias *I-V* characteristics of Al/SiO2/p-Si Schottky diodes shoved unusually linear behaviors in the intermediate bias between 0.1 V and 0.6 V in the temperature region of 295-400 K with an almost temperature independent slope. Experimental results show that the LnI-V characteristics MIS diodes exhibited unusually behaviors in intermediate bias region and in the studied with the slope of the Ln *I* vs *V* plot is almost temperature independent.The values of the ideality factor *n* controlled by the interface states density were found to be temperature dependent and it was found to change linearly with the 1/T. The plot of *kT/q*vs E_o(=nkT/q) and LnI_o values extracted from forward bias *I-V* characteristics showed a fairly linear behavior with the temperature indicated that the multistep tunnelling might be the possible carrier transport mechanism in our devices. The analysis of the temperature dependence of the forward bias *I-V* characteristics indicates that, at intermediate forward voltages, trap-assisted multistep tunnelling in the silicon space charge region is the mechanism that dominates the forward current. Also we have reported a modification which is includes the n and tunneling parameter $\alpha\chi^{0.5}\delta$ in the expression of reverse saturation current Io. This modification agrees with that obtained from the C-V data in literature, confirming the validity of the present approach.

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