

ANALYSIS OF TEMPERATURE DEPENDENT CHARACTERISTICS OF n-Al_{0.24}Ga_{0.76}As/GaAs STRUCTURES

A. BENĞİ, S.T. AGALIYEVA, S. ALTINDAL, S. ÖZÇELİK

*Physics Department,
Faculty of Arts and Sciences,
Gazi University, 06500, Ankara, Turkey,*

T.S. MAMMADOV

*Institute of Physics,
National Academy of Science,
AZ-1143, Baku, H.Javid ave., 33*

В температурном интервале 79-400К изучались, полученные из вольтамперных (*I-V*) характеристик, температурная зависимость электрических параметров n-Al_{0.24}Ga_{0.76}As/GaAs структуры. Передний наклон характеристики тока *I* оказался пропорциональным $I_0(T)\exp(AV)$, где *A* – наклон кривой Ln-V характеристики и не зависит от напряжения и температуры, $I_0(T)$ – относительно слабо зависящая от температуры функция. Полулогарифмическая Ln-V характеристика, основанная на механизме термоионной эмиссии (ТИ) показывает уменьшение фактора идеальности (*n*) и уменьшение нулевого наклона высоты барьера (Φ_{Bo}) с температурой. Такое поведение не подчиняется чисто теории термоионной (ТИ) эмиссии. Согласно экспериментальным данным мы считаем, что исследованный в настоящей работе, в температурном интервале 79-400К в механизме проводимости тока в нашей структуре доминирует многошаговое туннелирование через ловушки.

The temperature dependence of some electrical parameters of n-Al_{0.24}Ga_{0.76}As/GaAs structures obtained from the current-voltage (*I-V*) characteristics are studied in the temperature range of 79-400 K. The forward bias current *I* is found to be proportional to $I_0(T)\exp(AV)$, where *A* is the slope of Ln-*I-V* curves and almost independent of the voltage and temperature, and $I_0(T)$ is relatively weak function of temperature. The semi-logarithmic Ln-*V* characteristics based on the thermionic emission (TE) mechanism showed a decrease of the ideality factor (*n*) and increase of the zero-bias barrier height (Φ_{Bo}) with the increase of temperature. These behaviors not obey the pure thermionic emission (TE) theory. According to experimental data, we concluded that the current conduction mechanism of our sample in the temperature region of 79-400 K investigated in this work was predominated by a trap-assisted multistep tunnelling.

INTRODUCTION

In generally, the forward bias current-voltage (*I-V*) characteristics of metal-semiconductor (MS) or metal-insulator-semiconductor (MIS) contacts are linear on a semi-logarithmic scale at intermediate temperature and forward bias voltage but deviate considerably from linearity at low temperature ($T \leq 200$ K) due to the effect of series resistance R_s and the density of interface states N_{ss} . An increase in the value of ideality factor *n* due to interfacial insulator layer is well known and can be understood in terms of surface states which do not equilibrate with the metal and the potential drop across the insulator layer [3]. Due to the technological importance of such devices, there are a great number of studies have been made in last few decades [4-16]. The popularity of these studies, which is rooted in their importance to the semiconductor industry, does not assure uniformity of the results or of interpretation. Horvarth [4], independently from Card and Rhoderick [3], derived an expression for the ideality factor *n*, giving the contribution of the interfacial insulator layer and surface states to Schottky barriers lowering but forward and reverse bias and evaluated the interface state energy distribution and the relative interfacial insulator layer thickness. In addition, the characterization of R_s and N_{ss} in MS or MIS type Schottky diodes have become a subject of very intensive research and reported in the literature for more than four decades [2,3,5-7].

The high values of *n* ($n > 1$) were observed in several effects: (i) interface states at thin insulator layer between metal and semiconductor [16-18], (ii) tunnelling currents in highly doped semiconductors at low temperatures [19], (iii) image force lowering of the Schottky barrier in the high elec-

tric field at the metal-semiconductor interface [21], (iv) generation-recombination currents within the space-charge region [20]. A number of carrier transport mechanism such as thermionic emission (TE), thermionic field emission (TFE), minority carrier injection, recombination-generation and multi-step tunnelling compete, and usually one of them may dominate over the others in certain temperature and voltage region [22,23]. However simultaneous contribution from two or more mechanisms could also be possible.

In this work we report the results of systematic investigation on the temperature dependence of the electrical properties of MBE grown epitaxial Au/n-Al_{0.24}Ga_{0.76}As/GaAs structures. The forward bias *I-V* measurements of these structures were carried out over the temperature range 79-400 K. The main aim of this study is to present predominant carrier transport mechanisms. The analysis of the experimental data obtained for non-ideal Au/n-Al_{0.24}Ga_{0.76}As/GaAs structures indicated that the forward current transport is predominantly characterized by a multistep tunnelling mechanism at all temperatures used in this work.

EXPERIMENTAL PROCEDURE

The Au/n-Al_{0.24}Ga_{0.76}As/GaAs structure was grown by molecular beam epitaxy (MBE) technique. In MBE system, firstly 5000 Å undoped GaAs buffer layer was grown on Zn-doped (100) GaAs substrate. Then, Si-doped n-type 5000 Å Al_{0.24}Ga_{0.76}As and n-type Si doped GaAs epilayers were grown. Prior to ohmic and Schottky contact deposition, the sample was thoroughly cleaned and etched. The samples were dipped in methanol and deionized water sequentially for 10 min each for the removal of organic impurities from the

surface of the sample. It was then dipped in $H_2SO_4+H_2O_2+H_2O$ (1:1:300) for 5 s to remove the native oxide layer from the surface. Then the sample was inserted in a vacuum deposition chamber of the evaporator. Ohmic contacts of the electrodes were formed by evaporating Au in high vacuum ($P \cong 10^{-6}$ Torr) with 2000 Å thickness and subsequently annealing them for 90 minutes at 400 °C. After than the dot shaped contacts (rectifier) with area about 0.011 cm² and 2500 Å thickness were formed by evaporating of Au in high vacuum ($P \cong 10^{-6}$ Torr). In this way, Au/n-Al_{0.24}Ga_{0.76}As/GaAs structures were fabricated. The native interfacial insulator thickness δ was estimated to be about $\delta=47.3$ Å from measurement of the insulator capacitance in the strong accumulation region.

The forward and reverse bias current-voltage (*I-V*) characteristics of Au/n-Al_{0.24}Ga_{0.76}As/GaAs structures at various temperatures were measured in the temperature range of 79-400 K, using temperature controlled Janes 475 cryostat. Current-voltage (*I-V*) measurements of the prepared samples were performed using a Keithley 220 programmable constant current source and a Keithley 614 electrometer. The sample temperature was always monitored by using a copper-constantan thermocouple and a lakeshore 321 auto-tuning temperature controller with sensitivity better than ± 0.1 K.

RESULTS AND DISCUSSION

When a forward bias *V* is applied across the metal-semiconductor junction, *V* will be shared by the diode and series resistance. In this case, Thermionic emission (TE) model for the relationship between forward bias voltage and current of a Schottky diode can be written as follows [11].

$$I = I_o \exp\left(\frac{qV_d}{nkT}\right) \left[1 - \exp\left(-\frac{qV_d}{kT}\right)\right] \quad (1a)$$

where *I_o* is the reverse saturation current and described by

$$I_o = AA^* T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \quad (1b)$$

where the quantities *IR_s*, *A*, *A**, *T*, *q*, *k* and Φ_{Bo} are the terms is the voltage drop across series resistance of diode, the rectifier contact area, the effective Richardson constant, temperature in Kelvin, the electronic charge, Boltzman’s constant and the apparent barrier height at zero bias, respectively. The semi-logarithmic forward and reverse bias *I-V* characteristics of the Au/n-Al_{0.24}Ga_{0.76}As/GaAs structure at various temperatures, ranging from 79 to 400 K are shown in Fig.1. The saturation current *I_o* was obtained by extrapolating the linear intermediate voltage region of the part of linear curve to zero applied voltage and the Φ_{Bo} values were calculated from Eq.(1b) and the ideality factor values were obtained from the slope of forward bias *ln(I)-V* curves for each temperature as.

$$n = \frac{q}{kT} \frac{dV}{d \ln(I)} \quad (2)$$

In order to examine the dependence of *n* on temperature we plotted *n* versus 1000/*T* (Fig.2). It is seen from this figure that *n* changes with 1000/*T* linearly over the whole temperature range.

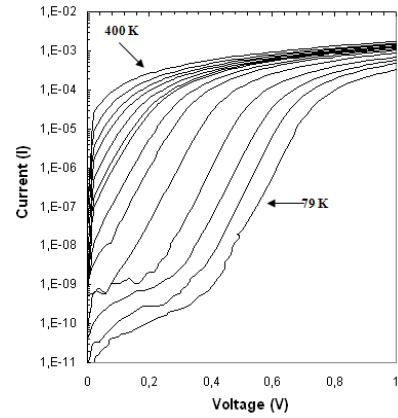


Fig.1. Forward bias *I-V-T* characteristics of the Au/n-Al_{0.24}Ga_{0.76}As/GaAs structure at various temperatures, ranging from 79 to 400 K.

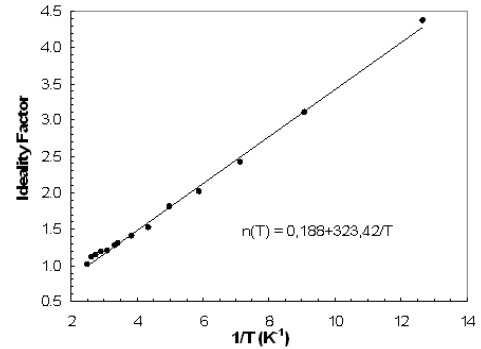


Fig.2. The ideality factor (*n*) versus inverse temperature (1/*T*) of the Au/n-Al_{0.24}Ga_{0.76}As/GaAs structure at temperature range of 79 -400 K.

The change in *n* with temperature may be represented by the following expression as

$$n(T) = \alpha + \beta / T \quad (3)$$

where the α and β are constant which were found to be 0.188 and 323.42 K respectively. The thermionic-field emission (TFE) mechanism can also be rule out in observed region, since *nT* is more or less constant in all temperature range. However, Padovani and Stratton [23] have pointed out that TFE could be responsible for current transport mechanism at moderate temperatures and doping levels. Obviously, since $E_{oo} \ll kT/q$ for our sample in the range of temperature used in this work, the possibility of the FE and TFE can easily be ruled out. In addition, the ideality factor *n* can be further analyzed by plotting *E_o* versus *kT/q*. Fig. 3 shows the experimental and theoretical (*n*=1) results of these plots. Experimental plots of *E_o* versus *kT/q* in Fig. 3 suggest that TFE may not be the process responsible for the current transport.

The slope of the *Ln I* vs *V* plot (Fig. 4) is almost temperature independent, with a value of approximately 31 V⁻¹. This behavior is quite suggestive of tunneling conduction mechanism in the Au/n-Al_{0.24}Ga_{0.76}As/GaAs structure dominating current flow through the junction. [24-26].

As can be seen in Fig. 4, the slope of *Ln I* vs *V* (Fig. 1) is almost constant with temperature. Also, the reverse saturation current depends slightly on temperature (Fig. 3) and diode ideality factor were found to be strongly dependent on temperature with *n*>1. We conclude that TE is not the limiting current transport mechanism in this voltage region.

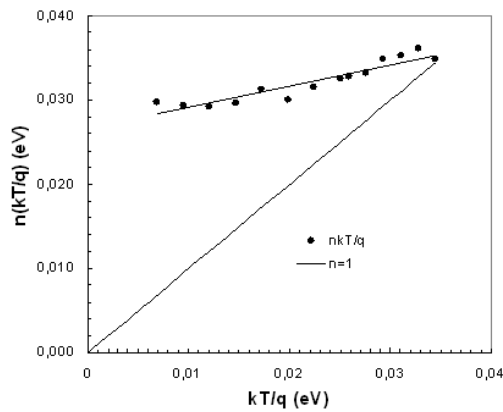


Fig.3. The n (kT/q) versus (kT/q) of the Au/n-Al_{0.24}Ga_{0.76}As/GaAs structure at temperature range of 79 -400 K.

Therefore it seems that trap assisted multistep tunnelling may be the mechanism that dominates the forward bias J - V characteristics in this voltage and temperature range for our samples. All these results have suggested that the tunnelling may play an important role in the current transport [24-27].

CONCLUSION

The forward bias I - V characteristics of Au/n-Al_{0.24}Ga_{0.76}As/GaAs structures were measured at wide temperature range (79-400 K). The forward bias semi-logarithmic \ln - V characteristics showed unusually linear behaviors in the intermediate biases with their slopes almost temperature independent.

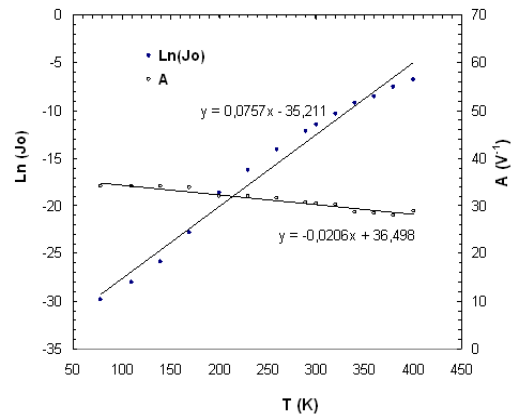


Fig.4. The slope of the $\ln I$ vs T plot and $\ln(I_o)$ vs T curves of the Au/n-Al_{0.24}Ga_{0.76}As/GaAs structure at temperature range of 79 -400 K.

The values of the ideality factor n controlled by the interface states density were found to be temperature dependent and it was found to change linearly with the inverse temperature. Experimental results indicating that the multistep tunnelling might be the possible carrier transport mechanism in our sample. In summary, the analysis of the temperature dependence of the dark I - V characteristics may suggest that, at intermediate forward voltages, trap assisted multistep tunnelling in the silicon space charge region may be the mechanism that dominates the forward current behaviors.

ACKNOWLEDGMENTS

This work is supported by Turkish of Prime Ministry State Planning Organization Project number 2001K120590 and Gazi University Scientific Research Project (BAP), FEF. 05/2005-48, 05/2006-05 and 05/2006-12.

[1]. Türüt, N. Yalçın, M. Sağlam, Solid State Electron., 35 (1992) 835.
 [2]. Ş. Altındal, S. Karadeniz, N. Tuğluoğlu, A. Tataroğlu, Solid State Electron., 47(10) (2003) 1847.
 [3]. H. C. Card, E. H. Rhoderick, J. Phys. D, 4 (1971) 1589. Zs. J. Horvarth, J. Appl. Phys., 63 (1987) 976.
 [4]. Singh, Solid State Electron., 28 (3) (1985) 223.
 [5]. S. Ashok, J. M. Borrego, R. J. Gutmann, Solid State Electron., 22 (1979) 621.
 [6]. W. M. R. Divigalpitiya, Sol. Energy Mater., 18 (1989) 253.
 [7]. Z. Quennoughy, Phys. Status Solidi A, 160 (1997) 127.
 [8]. J. Osvald, E. Burran, Solid State Electron, 42(2) (1998) 191.
 [9]. M. Depas, R. L. Van Meirhaeghe, W. H. Laflere, F. Cardon, Semicond. Sci. Technol., 7, (1992) 1476.
 [10]. E. H. Rhoderick, R. H. Williams, Metal Semiconductor Contacts, second ed. Clarendon Press, Oxford (1988).
 [11]. Türüt, M. Sağlam, H. Efeoğlu, N. Yalçın, M. Yıldırım, B. Abay, Physica B, 205 (1995) 41.
 [12]. H. A. Çetinkara, A. Türüt, D. M. Zengin, Ş. Erel, Appl. Surf. Sci., 207 (2003) 190.
 [13]. E. H. Nicollian, J. R. Brews, MOS Physics and Technology, Wiley, New York, 1982.
 [14]. S. M. Sze, Physics of Semiconductor Devices, second ed., New York (1981).
 [15]. H.C. Card, E.H. Rhoderick. J Phys D: Appl. Phys. 4 (1971) 1589.
 [16]. A.M. Cowley, S.M. Sze, J Appl Phys 36 (1965) 3212.
 [17]. Singh, K. C. Reinhardt, W.A. Anderson, J. Appl. Phys. 68 (1990) 3475.
 [18]. W.P. Kang, J.L. Davidson, Y. Gurbuz, D.V. Kerns, J. Appl. Phys. 78 (1995) 1101.
 [19]. P. Cova, A. Singh, Solid-State Electron 33 (1990) 11.
 [20]. W.M.R. Divigalpitiya, Solar Energ. Mater. 4 (1989) 253.
 [21]. A.N. Saxena, Surf. Sci. 13 (1969) 151.
 [22]. F.A. Padovani, R. Stratton, Solid. State Electron. 9 (1966) 695.
 [23]. A.R. Riben, D.L. Feucht, Int. J. Electron. 20 (1966) 583.
 [24]. Otto M, Neilsen J. Appl. Phys. 54 (1983) 5880.
 [25]. A.R. Riben, D.L. Feucht, Solid State Electron. 9 (1966) 1055.
 [26]. S. Ashok, P.P Sharma, S.J. Fonash, IEEE Trans On Electron Devices 27 (1980) 725.

Received: 10.02.2007