FREQUENCY AND TEMPERATURE DEPENDENT INTERFACE STATES AND SERIES RESISTANCE OF Au/CdTe SCHOTTKY DIODES

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Au/CdTe Şotki diodlarının 30 kHs-3MHs tezlik və 150-380K temperatur intervalında ğərğinlik tutumu $(C-V)$ və keçiriciliyin $\left(\Gamma/\omega-V\right)$ temperatur və tezlik asılılıqları tədqiq edilmişdir. Təcrübə xüsusilə kiçik tezliklərdə böyük tezlik dispersiyanin olduğunu və səth hallarının olması ilə əlaqədar mailin artdığını ğöstərdi. Nəticələr göstərdi ki, PTC qiymətləri C-V xarakteristikasının düz mailinin enmə əyrisində nəzərə çarpacaq dərəcədədir.

Исследованы частотные и температурные зависимости напряжения и емкости *(C-V)* и проводимости (*Γ / ω-V*) диодов Шотки Au/CdTe в температурном 150-380К и частотном диапазоне 30кГц -3МГц соответственно. Эксперимент показал довольно большую частотную дисперсию особенно в области низких частот, а также увеличение наклона из-за поверхностных состояний *Nss* в равновесии с полупроводником , что может приводит к избыточной емкости C-V и *Γ / ω-V* особенно в области низких частот . Результаты показали что значение PTC существенны только в низходящей кривизне прямого уклона характеристики *C-V* в области накопления и значение *Nss* являются существенными и в областях истощения и в инверсии.

The frequency and temperature dependent of capacitance-voltage (*C-V*) and conductance-voltage (*G/ω-V*) characteristics of the Au/CdTe Schottky diodes have been investigated by taking into account the effect of the series resistance (R_s) and interface states N_{ss} in the temperature range of 150-380 K and frequency 30 kHz -3 MHz, respectively. The experimental *C-V-f* and *G/ω-V-f* characteristics of Au/CdTe diodes show fairly large frequency dispersion especially at low frequencies and forward bias due to surface states N_{ss} in equilibrium with the semiconductor. The N_{ss} can easily fallow the ac signal especially at low frequency and yield an excess capacitance. The C–V and *G/ω-V* plots exhibit anomalous peaks due to the N_{ss} and R_s effect. Experimental results show that the values of R_s are significant only in the downward curvature of the forward bias *C-V* characteristics and accumulation region, but the values of N_{ss} are significant in both the inversion and depletion region.

1. INTRODUCTION

Metal/CdTe interfaces play an important role in optoelectronic devices. A clear understanding of the physical principles underlying the properties of these interfaces is therefore essential in order to develop practical devices based on this semiconductor material. The dominant charge transport mechanisms in Au/CdTe devices have been identified as thermionic emission over the barrier and space charge limited conduction [1-10]. There are several suggested methods [6-10], which could help to determination of the R_s, and among them the more important is the conductance technique developed by Nicollian and Goetzberger [10]. In the recent years, the frequency and temperature dependence of the *C-V-f/T* and *G/ω-V-f/T* characteristics of metal-semiconductor (MS) or metal-insulator-semiconductor (MIS) Schottky diodes [11-15] have been investigated considering interface states density N_{ss}, series resistance R_s and insulator layer effect. Among these works, a very interesting one is presented by Chattopadhyay and RayChaudhuri [16]. They have shown that, in the presence of a series resistance, the *C-V* characteristics should exhibit a peak. The peak value of the *C* and its position depend on the number of various parameters such as surface state density (N_{ss}), doping concentration (N_A), series resistance of device (R_s), and the thickness of the interfacial insulator layer (δ) [12,1516]. Both N_{ss} and R_s significantly influence the *C* and *G/ω* characteristics of the device from their ideal behavior and make the measured *C* and *G/ω* strongly frequency dependent. Therefore, it is important to include the effect of the frequency and to examine the details of frequency dispersion of capacitance peak.

In this work, our aim is to investigate experimentally the frequency and temperature dependence of forward and reverse bias *C-V* and *G/ω-V* characteristics for h of Au/CdTe diodes by considering the N_{ss} and R_s effects. The frequency and temperature dependence of interface states density was obtained from the *C-V* and *G/ω-V* measurements using the Hill-Coleman method [17]. Experimental results show that both N_{ss} and R_s are important parameters that influence the electrical characteristics of devices

2. EXPERIMENTAL PROCEDURE

Epitaxial layers of CdTe were grown on monocrystalline CdTe (111) substrate by photostimulated vapor phase epitaxy (PSVPE). Approximately a 5 μm epitaxial layers were deposited at 650 ºC with a 350 μm/h growth rate. In the growth, Cd source temperature was kept at 350 ºC for control to stoichiometry while CdTe source temperature was 750 ºC [13-15]. By controlling stoichiometry, the growth prosess makes it possible to obtain *n*-type epitaxial layers of CdTe. The CdTe wafers were cleaned by using standard cleaning method. Immediately after surface cleaning, high purity gold

(Au) metal (99.999 %) with a thickness of 1000 Å was thermally evaporated with a 2.2 Å/s grow rate onto the whole back surface of the wafer in the vacuum system. To form ohmic Au back contact, samples were temperature treatment at 400 ºC for 30 minutes in the vacuum system. After ohmic contact, circular dots of 1 mm indiameter and 1100 Å thick Au rectifying contacts were deposited onto CdTe surface. All evaporation processes were carried out in a turbo molecular fitted vacuum coating system (Bestek Technique) in the pressure of 10^{-8} mbar. The capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics of Au/CdTe Schottky barrier diodes were carried out with a HP 4192A LF impedance analyzer meter (5 Hz - 13 MHz) in the frequency and temperature range of 30 kHz-3 MHz and 150-380 K, respectively. A temperature controlled Janes 475 cryostat was used to allow electrical characteristics to be measured over a wide temperature range. The sample temperature was always monitored by using a Lakeshore-model 321 auto-tuning temperature controller with sensitively better than ±0,1K All measurements were carried out on the same sample to avoid the effect of the film thickness and performed under ($\leq 10^{-3}$ mbar) and in dark. In addition, these data were recorded using an IEEE-488 data acquisition system incorporated to a computer.

3. RESULTS AND DISCUSSIONS

The conductance technique [10,11] is based on the conductance losses resulting from the exchange of majority carriers between the interface states and majority carrier band of the semiconductor when a small ac signal is applied to the metal-insulator-semiconductor (MIS). The applied ac signal causes the Fermi level to oscillate about the mean positions governed by the dc bias, when the device is in the depletion. In Nicollian and Goetzberger's statically theory [10], the random distribution of discrete insulator charges and charged interface states in the metal/semiconductor interface plane cause a non-uniform distribution of surface band bending over the interfacial plane. To extract the series resistance of Schottky diode, several method have been suggested [8-11]. In our calculation we have applied the method developed by Nicollian and Goetzberger [10,11]. The real series resistance of the Au/CdTe Schottky barrier diodes can be subtracted from the measured capacitance (C_{ma}) and conductance (G_{ma}) in strong accumulation region at high frequencies (f ≥ 1 MHz) [10]. In addition, the voltage and frequency dependence of the series resistance profile can be obtained from the C-V and G/ω-V curves. To determine series resistance R_s, the MIS structure is biased into strong accumulation at sufficiently high frequency. The measured impedance (Z_{ma}) at strong accumulation of MIS or MOS structure using the parallel RC circuit [10] is equivalent to the total circuit impedance as

$$Z_{ma} = \frac{1}{G_{ma} + j\omega C_{ma}} \tag{1}$$

Comparing the real and imaginary part of the impedance, the series resistance is given by [22]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \tag{2}$$

where C_{ma} and G_{ma} represent the measured capacitance and conductance in strong accumulation region. The capacitance of insulator oxide layer C_{ox} is related to series resistance by

$$C_{ma} = \frac{C_{ox}}{(1 + \omega^2 R_s^2 C_{ox}^2)} \tag{3}$$

From this relation, C_{ox} is obtained as

$$C_{ox} = C_{ma}\left[1 + (\frac{G_{ma}}{\omega C_{ma}})^2\right] = \frac{\varepsilon_i \varepsilon_o A}{d_{ox}} \tag{4}$$

where, $\varepsilon_i = 3.8\varepsilon_o$ [23] and ε_o are the permittivities of the interfacial insulator layer and free space. Fig. 1(a) shows the temperature dependent *C-V* characteristics of the Au/CdTe Schottky barrier diodes. The values of capacitance, as shifting to forward bias region with decreasing temperature, give a peak in each temperature. The presence of the capacitance peak in the forward *C-V* plot is investigated by various experimental results on metal-insulator-semiconductor (MIS) [13,14,18] mainly due to the molecular restructuring and reordering of the interface states and series resistance. From the Fig. 1(a), it is shown that the change in the temperature has effects on the values and positions of these anomalous peaks. Fig. 1(b) shows temperature dependent *G/ω-V* characteristics of the Au/CdTe diode.

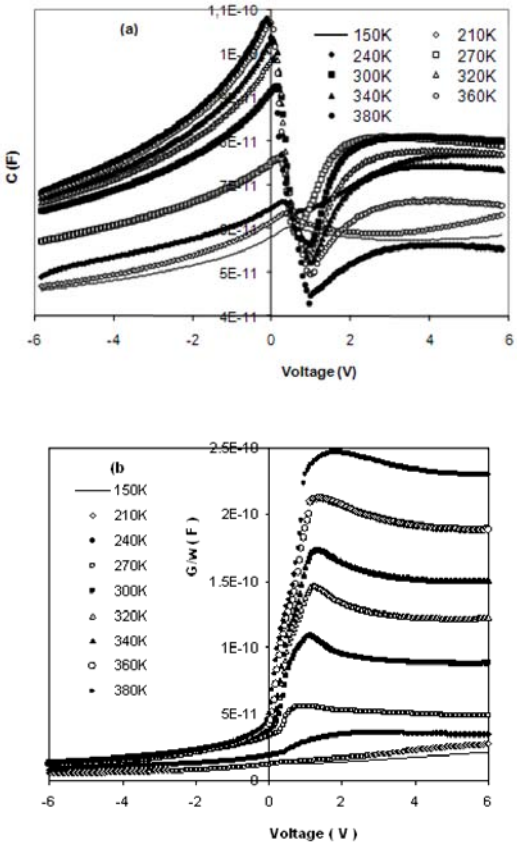

Fig. 1. The temperature dependent curves of: (a) the *C-V* and (b) *G/ω-V* characteristics of the Au/CdTe Schottky barrier diodes.

The real series resistance of Au/CdTe Schottky diodes can be obtained from the measured capacitance (C_m) and conductance (G_m) in strong accumulation layer at sufficiently high frequency (f≥1MHz). In addition the voltage and frequency dependence, series resistance can be obtained from the data in Fig. 1a and 1b[10]. The series resistance is calculated according to Eq.(2) and shown in Fig. 2 for various temperatures. These very significant values demanded that a special attention is given to the effects of series resistance in application of the admittance-based measurement methods (*C-V* and *G/ω-V*).

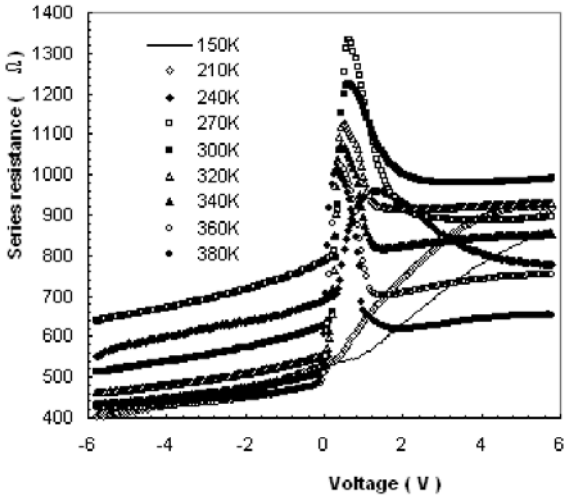

Fig.2. The temperature dependence of series resistance as a function of bias voltage for the Au/CdTe Schottky barrier diodes.

As seen in Fig. 2, the series resistances give the peaks in the voltage range of 0V≤ V ≤ 2 V. These peaks move to strong accumulation region with decreasing temperature. And the amplitude of these peaks increases with decreasing temperature. It is clearly seen that the series resistance depend on the changes in both temperature and voltage from region to region. These behaviors show that the trap charges have enough energy to escape from the traps located between metal and semiconductor interface in the CdTe band gap.

According to the Hill-Coleman [18], density of interface states is given by

$$N_{ss} = \left(\frac{2}{qA}\right)\frac{(G_m/\omega)_{\max}}{(G_m/\omega)_{\max} C_{ox})^2 + (1 - C_m/C_{ox})^2} \quad (5)$$

where, A is the area of the diode, ω is the angular frequency, C_m and $(G_m/\omega)_{\max}$ are the measured capacitance and conductance which correspond to peak values, C_{ox} is the capacitance of insulator layer. The values of various parameters for the Au/CdTe Schottky barrier diodes determined from *C-V* and *G/ω-V* characteristics in the temperature range of 150-380 K and frequency range of 30 kHz-3 MHz are given in Table 1 and Table 2, respectively.

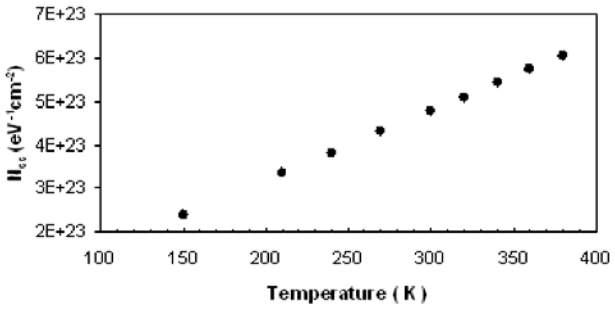

Fig. 3. Interface states density (N_{ss}) for various temperatures calculated from C-V and G/w-V measurements at 1 MHz.

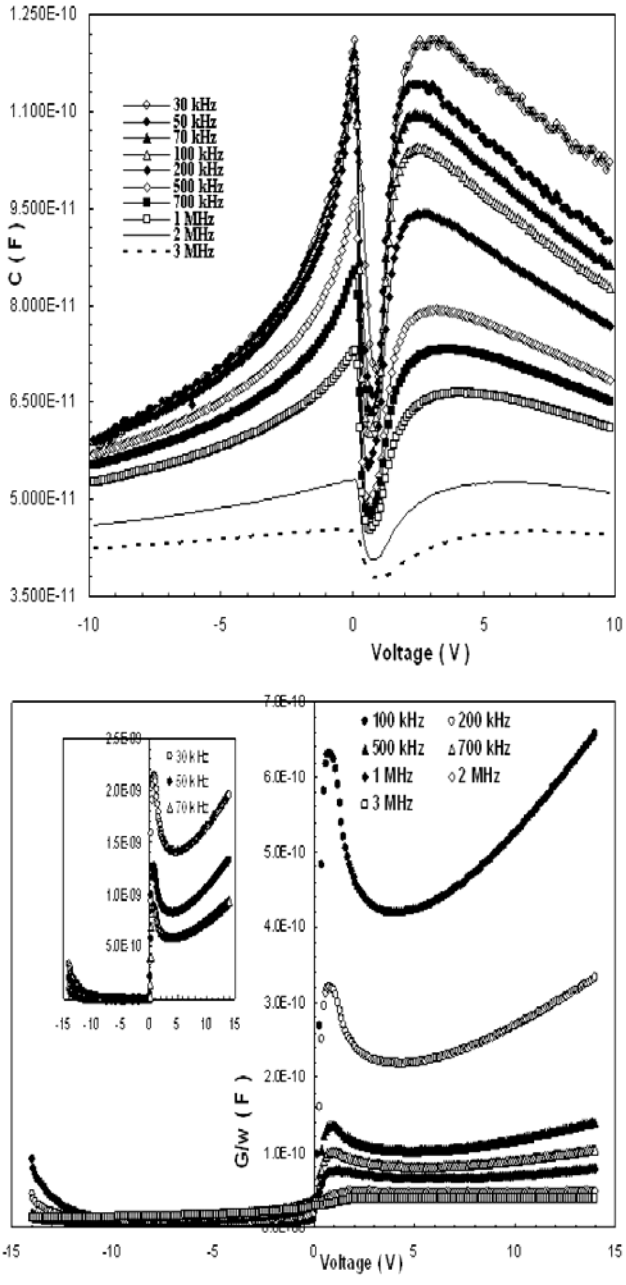

Fig. 4. The frequency dependent curves of: (a) the *C-V* and (b) *G/ω-V* characteristics of the Au/CdTe Schottky barrier diodes at room temperature.

Table 1.

The values of various parameters for Au/CdTe Schottky barrier diodes determined from *C- V* and *G/ω-V* characteristics in the temperature range of 150-380 K.

T (K)	V_m (V)	C_m (F)	G_m/w (F)	N_{ss} ($eV^{-1}cm^{-2}$)
150	0,40	6,03E-11	1,28E-11	2,17E+10
210	0,35	6,35E-11	1,46E-11	2,48E+10
240	0,30	6,62E-11	2,15E-11	3,66E+10
270	0,20	7,62E-11	3,54E-11	6,09E+10
300	0,15	9,24E-11	4,12E-11	7,21E+10
320	0,10	9,93E-11	4,17E-11	7,35E+10
340	0,05	1,03E-10	4,04E-11	7,15E+10
360	-0,05	1,07E-10	4,04E-11	7,18E+10
380	-0,10	1,08E-10	4,23E-11	7,52E+10

Table 2.

The values of various parameters for Au/CdTe Schottky barrier diodes determined from *C-V* and *G/ω-V* characteristics in the frequency range of 30 kHz-3 MHz.

F (kHz)	V_m (V)	C_m (F)	G_m/w (F)	N_{ss} ($eV^{-1}cm^{-2}$)
30	2,9	1,21E-10	1,47E-9	2.65E+12
50	2,8	1,14E-10	8,53E-10	1.53E+12
70	2,7	1,10E-10	6,12E-10	1.09E+12
100	2,6	1,04E-10	4,37E-10	7.74E+11
200	2,5	9,41E-11	2,30E-10	4.03E+11
500	3	7,92E-11	1,60E-10	2.76E+11
700	3,1	7,30E-11	8,43E-11	1.45E+11
1000	3,3	6,61E-11	6,76E-11	1.15E+11
2000	4	5,19E-11	4,68E-11	7.85E+10
3000	4,7	4,43E-11	3,84E-11	6.39E+10

The effect of density of interface states can be eliminated when the *C-V* and *G/ω-V* plots are obtained at sufficiently high frequency [10], since the interface states does not follow ac signal above this frequency. In this case, the series resistance that causes the non-ideal electrical characteristics of devices seems the most important parameter [10,12,13]. In order to see the frequency dependent *C-V* and *G/ω-V* characteristics, we plot the Fig. 3 which shows the experimental *C-V* and *G/ω-V* curves of the Au/CdTe Schottky barrier diodes in the frequency range from 30 kHz to 3 MHz at room temperature.

As seen Fig. 4(a) and (b), the low-frequency capacitance and conductance increases with applied voltage while the high-frequency capacitance and conductance remains almost constant. In other words, in the high frequency, the N_{ss} can not follow the ac signal and consequently do not contribute appreciably to the Au/CdTe Schottky barrier diodes capacitance. This situation may be different at low and intermediate frequencies, depending on the relaxation time of N_{ss} and the frequency of the ac signal [8-11]. As a result we can say that in the low frequencies N_{ss} can follow the ac signal and yield an excess capacitance and conductance, which depends on the frequency. But in the high frequencies ($f \geq 1$ MHz), the interface states can not follow the ac signal. This makes the contribution of interface state capacitance to the total capacitance negligibly small [10,12].

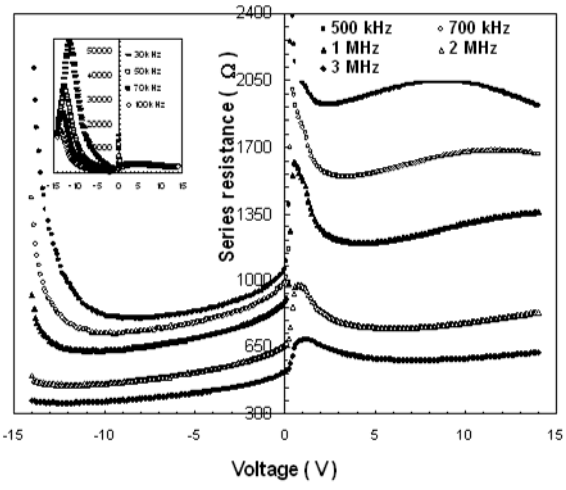

Fig.5. The frequency dependence of series resistance as a function of bias voltage for Au/CdTe Schottky barrier diode.

The peak values of capacitance especially at low frequencies have been found to be strongly dependent on the values of interface state density (N_{ss}) and series resistance (R_s). It can be explained that the N_{ss} can follow the ac signal and yield an excess capacitance and conductance, which depends on the relaxation time of N_{ss} and frequency of the applied ac signal. In this case the series resistance seems the most important parameter which causes the electrical characteristics of Au/CdTe Schottky barrier diodes to be non-ideal. As seen in Fig. 2, in the presence of a series resistance, the capacitance in the C-V plots has an anomalous peak for each temperature as in many studies[8-11].

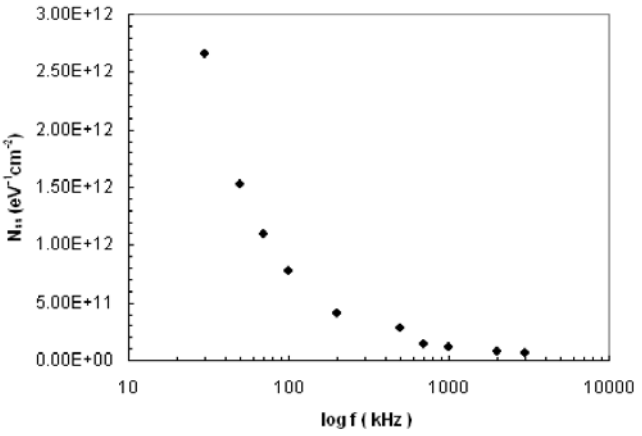

Fig.6. Interface states density (N_{ss}) for various frequencies calculated from C-V and G/w-V measurements at 300K.

CONCLUSION

To investigate the effects of the interface state density (N_{ss}) and series resistance (R_s) on the metal-ferroelectric-insulator-semiconductor Au/CdTe Schottky diodes, the *C-V* and *G/ω-V* characteristics of these structures are studied over a wide frequency and temperature range of 5 kHz-5 MHz and 150-380 K, respectively. Experimental result shows that both the *C-V* and *G/ω-V* characteristics are strongly frequency, temperature and voltage dependent and have peaks especially at low frequencies. Therefore, measured C-V and G/ω-V data at high frequencies were corrected for the effect of series resistance. This behavior of *C-V* and *G/ω-V* characteristics can be explained that the N_{ss} can follow the ac signal and yield an excess capacitance and conductance, which depends on the relaxation time of N_{ss} and frequency of the applied ac signal. The *C-V* and *G/ω-V* characteristics of the Au/CdTe Schottky diodes are found sensitive to temperature, especially at low temperature and forward bias due to the thermal restructuring and reordering of the interface. The frequency and temperature dependent C-V and G/ω-V characteristics confirm that the R_s and N_{ss} are important parameters that strongly influence the electric parameters in MIS structure.

ACKNOWLEDGEMENTS: This work is supported by Turkish of Prime Ministry State Planning Organization Project Number (BAB), FEF- Research Project FEF 05/2007-17 **,** DPT2001 K120590 and Gazi University BAP Research Projects 05/2005-53, 05/2006-12, 05/2006-05.

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Daxil olunub: 01.07.2007