Beynəlxalq Konfrans "Fizika-2005"
International Conference "Fizika-2005"
Международная Конференция "Fizika-2005"

7 - 9 İyun June Июнь 2005 №12 səhifə page стр. 63-68

Bakı, Azərbaycan Baku, Azerbaijan Баку, Азербайджан

# TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS OF $Au/Al_{0.24}Ga_{0.76}As/p$- GaAs STRUCTURES

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The forward bias current-voltage-temperature (*I-V-T*) and reverse bias capacitance-voltage-temperature (*C-V-T*) and conductance-voltage-temperature(G-W-T) characteristics of $Au/Al_{0,24}Ga_{0,76}As/p$- GaAs (PIN) structures are studied over a wide temperature range between 79 K and 400 K. Experimental results shows that the forward and reverse *I-V* characteristics show Schottky-junction-like behavior. The ideality factor *n*, series resistance $R_s$, barrier height $\phi_B$ and interface states $N_{ss}$ were found to be strong function of temperature. The *I-V* characteristics show non-ideal behavior with an ideality factor higher than unity especially at low temperature. The density of interface states distribution profiles as a function of ($E_{ss}$-$E_v$) deduced from the *I-V* measurements at different temperatures for the sample on the order ~$10^{13}$ $cm^{-2}.eV^{-1}$. While the *n*, $R_s$ , $N_{ss}$ decrease, the zero-bias barrier height $\phi_{B0}$ increase with increasing temperature. In addition to the value of series resistance $R_s$ obtained as function voltage and temperature from *C-V G-V* characteristics. Experimental results show that the performance of the $Au/Al_{0.24}Ga_{0.76}As/p$- GaAs structures has been found to be sensitive to the $R_s$ and $N_{ss}$.

## 1. INTRODUCTION

The characterization of interface states and series resistance in $Au/Al_{0.24}Ga_{0.76}As/p$-GaAs type structures have become a subject of very intensive research and reported in the literature for more than four decades [1-4]. When the devices have a $R_s$, which causes the voltage drop across the junction to be less than the applied voltage between the terminals of the structure. Especially, forward bias current-voltage (*I-V*) and admittance (*C-V* and *G-V*) characteristics at high voltages deviate considerably from ideal behavior due to the effect of parameters such as the $R_s$ and $N_{ss}$ [5-9]. In this study, the fabrication parameters and temperature dependent current-voltage (*I-V*) and admittance-voltage (*C-V, G-V*) characteristics of the $Au/Al_{0.24}Ga_{0.76}As/p$-GaAs structures at wide temperature range (79-400 K) are reported. In addition, we investigate the effects of the $N_{ss}$ and $R_s$ behavior an electrical characteristics of these device, and we report results of a systematic investigation on the voltage and temperature dependence of the electrical properties of the $Au/Al_{0.24}Ga_{0.76}As/p$-GaAs structures. In order to achieve a good understand these effects, we measured the admittance characteristics in wide temperature range (79-400 K) and voltage range (-6V, 6V).

## 2. EXPERİMENTAL DETAİLS

In $Al_{0.24}Ga_{0.76}As/p$-GaAs structure, 5000 Å undoped buffer layer was growth on Zn-doped (100) GaAs substrate. Then, Si-doped n-type 5000Å $Al_{0.24}Ga_{0.76}As$ and n-type Si doped GaAs epilayers was growth. Ohmic contacts of the electrodes were formed by evaporating Au in high vacuum (P=$10^{-6}$ Torr) with 2000 Å thickness and subsequently annealing them for 90 minutes at 400 ºC. After than the Schottky contacts (rectifier) were formed by evaporating of Au dots with area about 0.011 $cm^2$ with 2500 Å thickness in high vacuum(P=$10^{-6}$ Torr). The current-voltage (*I-V*), capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics of $Au/Al_{0.24}Ga_{0.76}As/p$-GaAs structures at various temperatures were measured in the temperature range of 79-400 K using temperature controlled Janes 475 cryostat.

The *I-V* characteristics of the prepared samples were performed using a Keithley 220 programmable constant current source and a Keithley 614 electrometer. The *C-V* and *G-V* characteristics were performed at 100 kHz by using HP 4192A LF impedance analyzer (5 Hz-13 MHz).

## 3. RESULT AND DISCUSSION

### *3.1. The temperature dependent of forward bias current-voltage(I-V) characteristics*

For a Schottky barrier diode, the barrier height, the forward bias current-voltage *(I-V)* relation obtained by using thermionic emission (TE) theory is given by [5,6]

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right] \quad (1)$$

where $V$ is the forward bias voltage (V), $n$ is the ideality factor, $R_s$ is the series resistance, $I_o$ is the reverse saturation current (A) and obtained by extrapolating the linear intermediate voltage region of the curve to zero applied voltage and is given

$$I_0 = AA^*T^2 \exp\left(\frac{q\Phi_{bo}}{kT}\right) \quad (2)$$

where $A$ is the diode area ($cm^2$), $A^*$ is the effective Richardson constant of 3 A $cm^{-2}$ .$K^{-2}$ for p-type GaAs and $\phi_{B0}$ is the zero-bias barrier height (eV). From Eq. (1), diode ideality factor $n$ can be written as: n=q/kT(dV/dLn(I)). The term of *dV/dLnI* is the slope of linear region of *I-V* plots. The forward bias semi-logarithmic *LnI-V* characteristic for one of the $Au/Al_{0.24}Ga_{0.76}As$/p- GaAs structures in the temperature range from 79-400 K are shown in Fig. 1. Each curve consist of a linear range with different slopes in intermediate bias regions (0.05V≤V≤0.55V) showing the exponential relationship between the current and voltage (*I-V*).

The zero-bias barrier height $\phi_{B0}$ and diode ideality factor $n$ values were calculated from Eq. (2), and shown in Table 1. The zero-bias barrier height $\phi_{B0}$ and diode ideality factor $n$ values were calculated from Eq. (2), and shown in Table 1. As shown in Table 1, the $\phi_{B0}$ and $n$ determined from semilog-forward *I-V* plots were found to be a strong function of temperature (especially at low temperatures). The ideality factor $n$ was found to decrease, while the $\phi_{B0}$ increase with increasing temperature ($n$=4.420 and $\phi_{B0}$=0.276 eV at 79 K, $n$=1.02 and $\phi_{B0}$=0.726 eV at 400K). Similar results have been reported in the literature [7,8,10]. The values of the diode ideality factor $n$ as obtained here indicate that the current transport mechanism consists of both the trap-assisted tunneling and the thermionic emission. Nagatomo et. al. [11] reported that the variation of the diode ideality factor corresponds to the performance of this type structure. The barrier height values $\phi_{B0}$ calculated from *I-V* characteristics shows an unusual behaviour that it increases with the increase of temperature.

Table 1. Temperature dependent values of various parameters determined from *I-V* characteristics of $Au/Al_{0,24}Ga_{0,76}As$/p- GaAs structures.

| T (K) | $I_o$ (A) | n | $\Phi_{B0}$(I-V) (eV) | $n\Phi_{B0}$(I-V) (eV) |
|---|---|---|---|---|
| 79 | 1.44E-15 | 4.42 | 0.276 | 1.22 |
| 110 | 6.03E-13 | 3.27 | 0.333 | 0.989 |
| 140 | 9.38E-15 | 2.36 | 0.480 | 1.180 |
| 170 | 7.63E-14 | 2.01 | 0.550 | 1.100 |
| 200 | 6.01E-11 | 1.76 | 0.547 | 0.960 |
| 230 | 1.31E-09 | 1.55 | 0.573 | 0.888 |
| 260 | 9.36E-09 | 1.44 | 0.609 | 0.876 |
| 290 | 8.72E-08 | 1.40 | 0.629 | 0.880 |
| 300 | 1.26E-07 | 1.32 | 0.643 | 0.848 |
| 320 | 4.23E-07 | 1.30 | 0.656 | 0.852 |
| 340 | 1.1E-06 | 1.27 | 0.673 | 0.854 |
| 360 | 3.54E-06 | 1.17 | 0.680 | 0.790 |
| 380 | 6.33E-06 | 1.06 | 0.702 | 0.744 |
| 400 | 1.01E-05 | 1.02 | 0.726 | 0.740 |

Such temperatures dependence is an obvious disagreement with reported negative temperature coefficient of the barrier height. However, the barrier height $\phi_B(C-V)$ determined from $C^{-2}$ vs. $V$ plot at high frequency decreased linearly with the temperature(Fig. 2.). There is a consistent disagreement between the values of $\phi_{B0}(I-V)$ and $\phi_B(C-V)$. While the zero-bias barrier height $\phi_{B0}$ increases, the ideality factor $n$ decreases with an increase in temperature; the changes are quite significant especially at low temperatures due to the large leakage current, which may be contributed to the large amount of patch with low barrier height.

The effective barrier height $\phi_e$ is given as[8]

$$\phi_e = \phi_B + \left(1 - \frac{1}{n(V)}\right)(V - IR_S) \quad (3)$$

by considering the applied voltage dependence of barrier height. If the $Au/Al_{0,24}Ga_{0,76}As$/p- GaAs structures having interface states $N_{ss}$ in equilibrium with the semiconductor, the ideality factor $n$ becomes greater than unity, as proposed by Card and Rhoderic [9], is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{W_D} + N_{ss}(V)\right) \quad (4)$$

In the p-type semiconductors, the energy of interface states $E_{ss}$ with respect to the top of the valance band at the interface of semiconductor is given by [12], is

$$E_{ss} - E_V = q(\phi_e - V) \qquad (5)$$

where $\phi_e$ is assumed to be bias- dependent due to the presence of an interfacial layer and interface states located at the interfacial insulator layer- semiconductor interface.

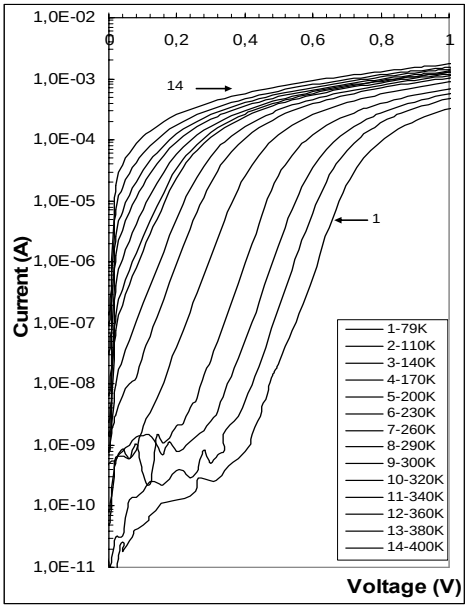


Fig. 1. The forward bias and reverse bias *I-V* characteristics of $Au/Al_{0,24}Ga_{0,76}As/p$- GaAs structures at different temperatures.

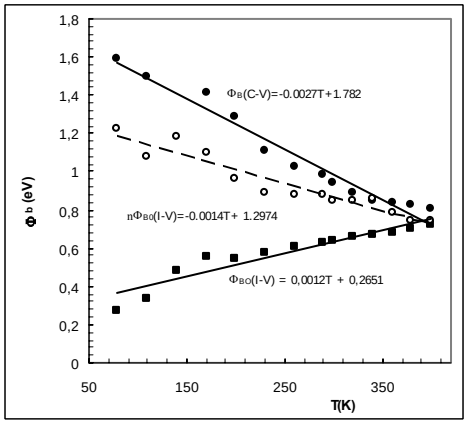


Fig.2. The $\phi_{B0}(I-V)$ vs T and $\phi_B(C-V)$ vs T plots for $Au/Al_{0.24}Ga_{0.76}As/p$-GaAs structure

The $\phi_e$ is given as:

$$\phi_e = \phi_B + \left(1 - \frac{1}{n(V)}\right)(V - IR_S) \qquad (6)$$

by considering the applied voltage dependence of barrier height. If the $Au/Al_{0.24}Ga_{0.76}As/p$-GaAs structures having interface states $N_{ss}$ in equilibrium with the semiconductor, the ideality factor $n$ becomes greater than unity, as proposed by Card and Rhoderic [9], is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{W_D} + N_{ss}(V)\right) \qquad (7)$$

where $\varepsilon_i$ and $\varepsilon_s$ are the permittivities of interfacial insulator layer and semiconductor, respectively, $W_D$ in the space charge with and $N_{ss}$ is the density of interface states in equilibrium with semiconductor. The temperature dependent energy distribution of the $N_{ss}$ was determined from experimental forward bias *I-V* measurement and given in Fig. 3. The values of $R_s$ for each temperature were obtained from *C-V* and *G-V* measurement as explained in section 3.2. Thus, we have obtained temperature dependent density distribution profile of the interface states as a function of $E_{ss}$-$E_V$ and are shown in Fig. 3. We have observed than that the mean $N_{ss}$ decrease with increasing temperature. Such mean behaviour is attributed the molecular restructuring and reordering of insulator-semiconductor interface under the temperature effect [13]. As can be seen from Fig. 3., for all temperature, a slight experimental rise of the $N_{ss}$ from mid gap towards of the valance band and $N_{ss}$ curves have a minimum especially at low temperatures.

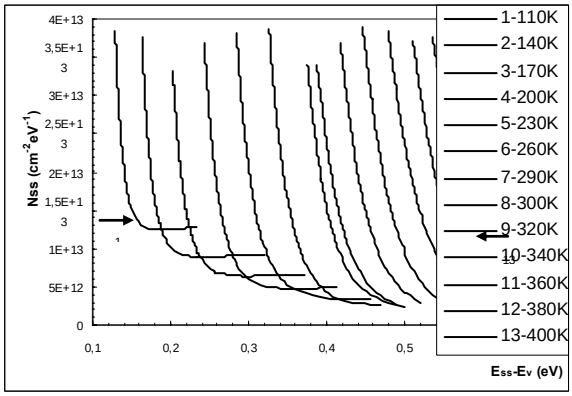


Fig.3 .The $N_{ss}$ versus of $E_{ss}$-$E_v$ deduced from the *I-V* data at different temperatures for $Au/Al_{0.24}Ga_{0.76}As/p$-GaAs structure.

*3.2. C-V/T and G-V/T characteristics*

The differential capacitance measurements at 100 kHz under reverse bias were performed at the different temperatures over the range of 79-400 K. The typical $C^{-2}$ vs $V$ curves are shown in Fig. 4 and the curves show excellent linearity. As shown in Fig. 4, $C^{-2}$ vs $V$ plots at 100 kHz for each temperature are linear over the voltage range -1.5V≤V≤-0.5V. This linear behavior of $C^{-2}$ vs $V$ plots shows that the measurements are made at sufficiently high frequency ($\omega$), such that carrier lifetime ($\tau$) is much larger than $1/\omega$, the change in interface states cannot follow a.c.signal [5,7,14]. The linear plot is very useful for analyzing the experimental *C-V* characteristics. The $C^{-2}$ vs $V$ characteristics can be described by [5]

$$C^{-2} = \frac{2}{q\varepsilon_s A^2 N_A}(V_0 + V) \qquad (8)$$

where $A$ is the area of the cells, $\varepsilon_s$ in the permittivity of semiconductor, $N_A$ is the carrier doping density of acceptors and $V_0$ is the intercept of $C^{-2}$ with the voltage axis and is given by

$$V_0 = V_D + kT/q \qquad (9)$$

The barrier height from the inset of Fig. 7 and Table.2 as

$$\phi_B(C-V) = V_D + E_F - \Delta\phi_B \qquad (10)$$

where, $V_D$ is the diffusion potential, $\Delta\phi_B$ is the image force barrier lowering, $E_m$ is the maximum electric field and $E_F$ is the energy difference between the bulk Fermi level and valance band edge given by [5]. The temperature variation of $\phi_B(C-V)$ can be readily calculated with the use of following standard relations:

$$E_F = \frac{kT}{q} Ln(N_V / N_A) \qquad (11)$$

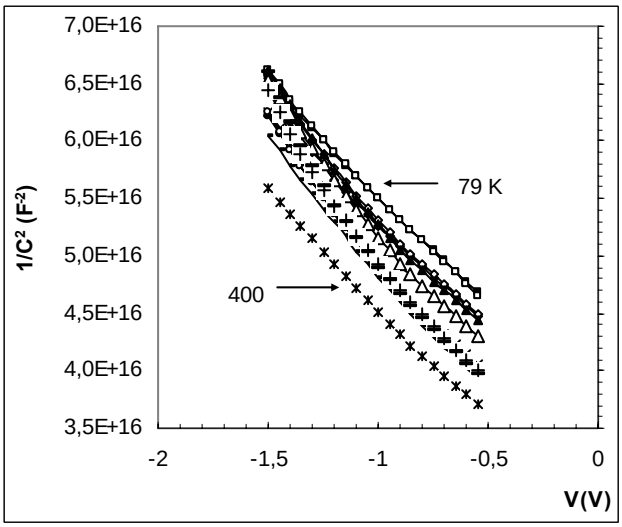


Fig. 7. The $C^{-2}$ vs $V$ of $Au/Al_{0,24}Ga_{0,76}As/p$- GaAs structure for different temperatures at frequency of 100 kHz.

where $N_V$ is the effective density of states in p-GaAs valance band. The values of $N_A$, $E_F$, $V_D$, $W_D$ and $\Delta\phi_B$ determined from $C^{-2}$ vs $V$ curves at different temperatures are listed in Table 2, respectively. The temperature dependent of barrier height $\phi_B(C-V)$ are calculated from the corresponding values of $V_B$, $E_F$, $\Delta\phi_B$ are shown in Table 2. We found from the measurement C-V data the barrier height $\phi_B(C-V)$ decreases almost linearly with temperature as

$$\phi_B(C-V) = \phi_{B(C-V)}(0K) + \alpha T \qquad (12)$$

Here the barrier height at absolute zero $\phi_{B(C-V)}(0K)$ and temperature coefficient of the barrier height $\alpha$ are experimentally found to be 1.78 eV and $-0.27\times10^{-4}$eV/K, respectively. Here the negative temperature coefficient of the barrier height is found to be very close of the GaAs band gap of $\sim8.5\times10^{-4}$eV/K. Similar results have been reported with $\alpha$-values of $2\times10^{-4}$ eV/K [5,12]. Experimental result shows that the value of $\phi_{B(C-V)}(0K)$ is found to be greater than $\Phi_{B0}$(I-V) by the ideality factor at each temperature. If it is accepted that $\phi_{B(C-V)}(0K)$ data are the most reliable, as found by Bhuiyan [16], we can define a term

$$\Phi_B(T) = \Phi_B(C-V) = n(T)\Phi_{B0}(I-V) \qquad (13)$$

called the true barrier height in I-V measurements.

Table 2. Temperature dependent values of various parameters determined from *C-V* characteristics of $Au/Al_{0,24}Ga_{0,76}As/p$- GaAs structure

| T (K) | $N_A$ ($cm^{-3}$) | $E_F$ (eV) | $V_D$ (V) | $W_D$ (cm) | $\Phi_B$(C-V) (eV) |
|---|---|---|---|---|---|
| **79** | 4.771E+18 | 2.612E-03 | 1.801 | 1.696E-06 | 1.803 |
| **110** | 4.660E+18 | 3.860E-03 | 1.739 | 1.716E-06 | 1.742 |
| **140** | 4.644E+18 | 6.016E-03 | 1.619 | 1.719E-06 | 1.625 |
| **170** | 4.362E+18 | 8.158E-03 | 1.486 | 1.773E-06 | 1.494 |
| **200** | 4.131E+18 | 1.046E-02 | 1.340 | 1.822E-06 | 1.35 |
| **230** | 4.021E+18 | 1.243E-02 | 1.237 | 1.847E-06 | 1.249 |
| **260** | 4.063E+18 | 1.361E-02 | 1.165 | 1.837E-06 | 1.179 |
| **290** | 4.721E+18 | 1.019E-02 | 1.298 | 1.705E-06 | 1.309 |
| **300** | 4.197E+18 | 1.412E-02 | 1.184 | 1.808E-06 | 1.198 |
| **320** | 4.008E+18 | 1.636E-02 | 1.127 | 1.850E-06 | 1.143 |
| **340** | 3.959E+18 | 1.770E-02 | 1.093 | 1.862E-06 | 1.111 |
| **360** | 3.752E+18 | 2.044E-02 | 1.006 | 1.912E-06 | 1.026 |
| **380** | 3.520E+18 | 2.371E-02 | 0.872 | 1.974E-06 | 0.896 |
| **400** | 4.771E+18 | 2.612E-03 | 1.801 | 1.696E-06 | 1.803 |
| **380** | 4.660E+18 | 3.860E-03 | 1.739 | 1.716E-06 | 1.742 |
| **400** | 4.644E+18 | 6.016E-03 | 1.619 | 1.719E-06 | 1.625 |

*3.2.1 Temperature and voltage dependent series resistance*

The *C-V* and *G-V* measurements at 100 kHz were performed at the different temperature at the range of 79-400 K. Before any analysis could take place, all the measurements must be corrected for series resistance and it is very important parameter of Au/AlGaAs/p-GaAs structure. Therefore, the values of $R_s$ are calculated from the measured admittance when the structures are biased in strong accumulation [7,14,15]. In addition to V dependence of the series resistance can be obtained from the measurements of *C-V* and *G-V* curves. According to [14]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \left(\omega C_{ma}\right)^2} \qquad (14)$$

where $C_{ma}$ and $G_{ma}$ represent the measured capacitance and conductance in strong accumulation region. All the measurements were corrected for series resistance measurements. This resistance evolves from non-ideal contacts on the device. Measured series resistance $R_s$ vs applied voltage with temperature as a parameter for a signal frequency of 100 kHz are shown in Fig. 5. As shown in Figure. 5. the values of Rs change region to region with applied voltage and temperature.

Especially, while the values of series resistance decreases with increasing temperature in accumulation region, increase with increasing temperature in depletion and reverse regions. The values of series resistance $R_s$ give two peaks at reverse and forward bias about between -4V≤V≤-1V and 0V≤V≤1.5V, respectively. These peaks shifted to accumulation region with decreasing temperature and amplitude of peaks increased with increasing temperature in the *C-V* and *G-V* measurements. Such behaviour of the series resistance have been attributed to particular distribution of interface states [7,15]. As shown in Fig. 5, the values of series resistance showed a strong dependence on the applied voltage at various temperatures.

## 4. CONCLUSION

The *I-V-T* and *C-V-T* and *G-V-T* characteristics of $Au/Al_{0.24}Ga_{0.76}As/p\text{-}GaAs$ structure were measured in temperature range of 79-400 K. It is well known both the presence of Nss and Rs are the important parameters which caused the ideality. Therefore, these basic parameters of $Au/Al_{0,24}Ga_{0,76}As/p\text{-}GaAs$ structure were determined a wide temperature and voltage range of 79-400 K and -6V to 6V, respectively. The n, $R_s$, $\phi_B$ and $N_{ss}$ were found to be strong function of temperature. While *n*, $R_s$ and $N_{ss}$ decrease, $\phi_{B0}$ increase with increasing T. The $N_{ss}$ decreases with increasing temperature. This behaviour is the result of atomic restructuring and reordering at the metal-semiconductor interface. In addition to, there are a disagreement between the $\phi_B(C-V)$ measurements and those determined from *I-V* data ($\phi_{B0}$). This discrepancy between *C-V* and *I-V* determined barrier height could be explained by assuming a Gaussian distribution of barrier height with a main value $\overline{\phi}_{B0}$ and a standard deviation $\sigma_s$. In the other words, for the discrepancy between the *I-V* and *C-V* measured Schottky barrier height can be explained as the current in the *I-V* measurements is dominated by the current which flows through the region of low Schottky barrier.

**Acknowledgements:** This work is supported by Turkish of Prime Ministry State Planning Organization project number 2001K120590.

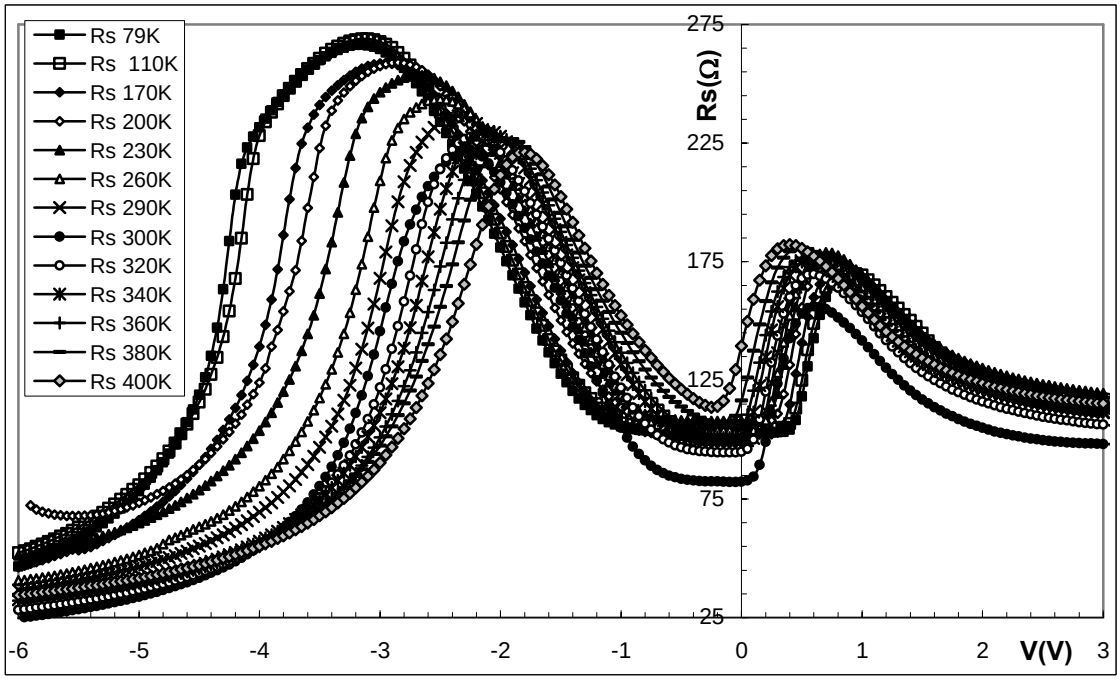


Fig.5. The $R_s$ vs *V* plot of $Au/Al_{0.24}Ga_{0.76}As/p\text{-}GaAs$ structure at different temperature.

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