Beynəlxalq Konfrans "Fizika-2005"
International Conference "Fizika-2005"
Международная Конференция "Fizika-2005"

7 - 9 İyun / June / Июнь 2005 | №13 | səhifə / page / стр. 69-74

Bakı, Azərbaycan | Baku, Azerbaijan | Баку, Азербайджан

THE GROWTH OF $Al_xGa_{1-x}As$/GaAs NANOSTRUCTURES WİTH MBE METHOD AND THE INVESTİGATİON OF ELECTROPHYSİCAL PROPERTİES

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In this work $Al_xGa_{1-x}As$/GaAs p-i-n diode structure was growth with SEMİCON VG80H MBE device. In this structure, 0.5 μm undoped i-type GaAs buffer layer, 0.5 μm Si-doped n-type $Al_{0.24}Ga_{0.76}As$/GaAs layer and 500A Si-doped n-type GaAs epilayer growth on Zn-doped (100) p-type GaAs substrate in order. For results and analysis of layer thicknesses and x concentration; x-ray diffraction and LEPTOS simulation methods was used. I-V and C-V measurements were taken. In addition to structural analysis of this structure, we investigated the effect of series resistance R_s and interface state density N_{ss} on the I-V and C-V characteristics. Experimental results show that the downward concave curvature of the forward bias I-V plot at sufficiently high voltages is caused by the Rs and Nss. Therefore the Nss distribution profile and Rs were obtained the forward bias I-V characteristics for prepared this structures at room temperature. The mean density of Nss estimated from the room temperature I-V measurements by taking into account the bias dependence of effective barrier height was $\cong 10^{13} cm^{-2} eV^{-1}$.

1. INTRODUCTION

Recently, producing high quality optoelectronic devices, $A^{III} B^{V}$ based heterostructures used mostly. The schottky diodes, field effect transistors(FET) and the injection lasers having low current density are prepared from GaAs and AlGaAs based nanodimensional heterostructures [1-3]. Currently in the producing of nanodimentional quant wells and quant dots, molecular beam epitaxy (MBE) is used rather than other growth techniques [4-6]. Some fundamental works in electronic industry are currently focusing on metal/GaAs contacts. Recently, the I-V and C-V characteristics of metal-semiconductor (MS) or metal-insulator-semiconductor(MIS) type Schottky diodes have been subject of intensive work [7-10]. In particular, considering the effect of the Rs and Nss, has been investigated [9-11]. A number of works which suggested various ways of determining the interface parameters and of understanding the nature of the Nss and Rs have carried out a considerable amount to work. Card and Rhoderic [12] obtained a general expression for the ideality factor (n) of the forward bias I-V characteristics. Cheung and Cheung [13] obtained a new expression, to obtained Schottky diode parameters suggest n, Φ_B and R_s.

The current-voltage (*I-V*), capacitance-voltage (*C-V*) characteristics of $Al_{0.24}Ga_{0.76}As$/p-GaAs p-i-n diode and $Al_{0.2}Ga_{0.8}As$/GaAs MQW Structure at room temperature were measured. The *I-V* characteristics of these structures were performed using a Keithley 220 programmable constant current source and a Keithley 614 electrometer. The *C-V* characteristics were performed at 100 kHz by using HP 4192A LF impedance analyzer (5 Hz-13 MHz). The aim of this work is to experimentally investigate the effect of Rs and Nss on the non-ideal I-V characteristics for prepared $Al_xGa_{1-x}As$/GaAs structures at room temperature. The other purpose this study, in order to extract the values of the n, Φ_B and R_s of these structures, Cheung's method [12] has been applied in the room temperature

2. EXPERIMENTAL PROCEDURE

2.1 The growth of $Al_{0.24}Ga_{0.76}As$/GaAs PIN diode structure with MBE

Firstly, Zn-doped (100) p-type GaAs substrate was heated to 400 ºC by 0.2ºC/s increment factor. Than the

substrate temperature was increased to 690 ºC by 0.1ºC/s increment factor. Removal of oxide layer was observed with RHEED. After this process substrate temperature was lowered to 640 ºC, the growth temperature. After this, 5000 Å undoped i-type GaAs buffer layer was growth firstly with 2.78 Å/s growth rate. Then 0.5 µm n-type $Al_{0.24}Ga_{0.76}As$ ($n_{Si}=5*10^{17}$ cm^{-3}) layer was growth with 0.447 Å/s growth rate for AlAs and 0.67 Å/s growth rate for GaAs. Then 500 Å Si-doped n-type GaAs ($n_{Si}=1*10^{18}$ cm^{-3}) doped epilayer was growth with 2.78 Å/s growth rate. Lastly, substrate temperature was decreased to 400 ºC with 0.1 ºC/s steps. Structure of p-i-n diode and Ga, Al, As, Si fluxes and Al concentration in growth process was given in Fig.1 and 2.

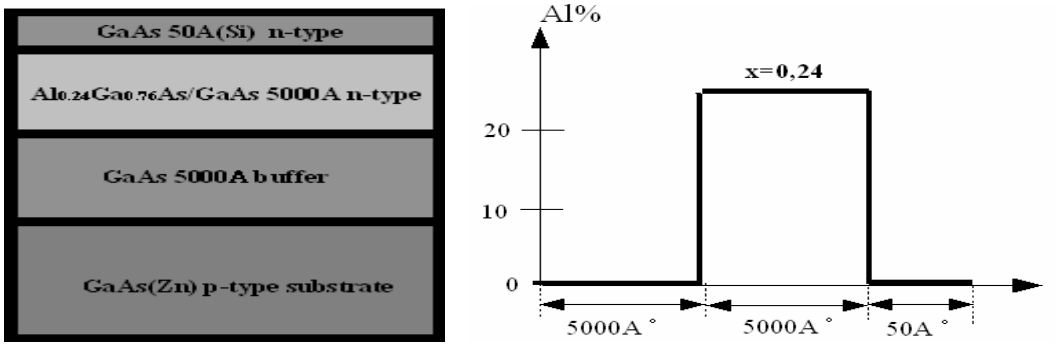


Fig.1. The structure of $Al_{0.24}Ga_{0.76}As$/GaAs PIN diode

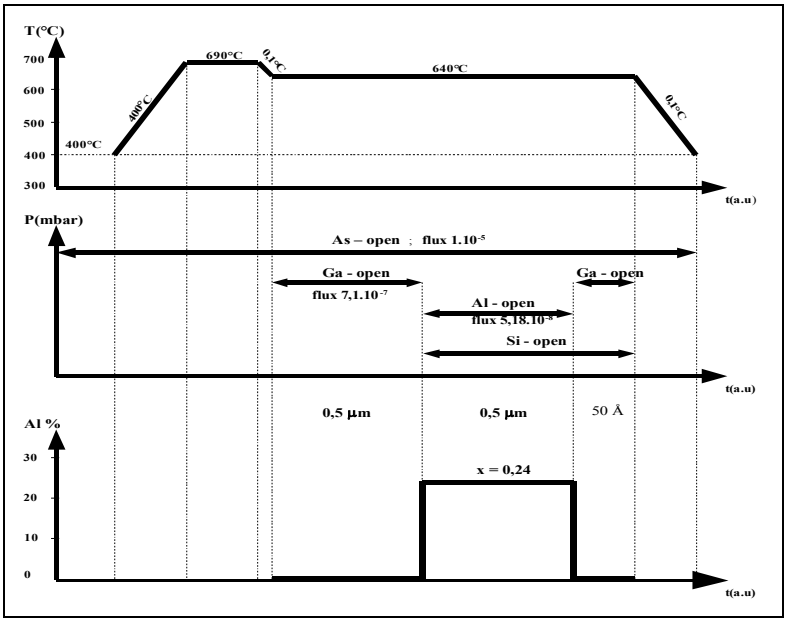


Fig.2. Ga,Al,As,Si fluxes and Al concentration in growth process for $Al_{0.24}Ga_{0.76}As$/GaAs p-i-n diode

2.2 $Al_{0.2}Ga_{0.8}As$/GaAs MULTI QUANTUM WELL (MQW) STRUCTURE

In $Al_{0.2}Ga_{0.8}As$/GaAs structure, 5000 Å buffer layer was growth on Zn-doped (100) GaAs substrate. Then, 20-period MQW which has 250 Å $Al_{0.2}Ga_{0.8}As$ and 50 Å undoped GaAs layers in each period, was growth. The growth rate of AlAs and GaAs in the MQW structure, is the same was in the growth rates of the p-i-n structure. The schema of the growth MQW structure was given in Fig.3.

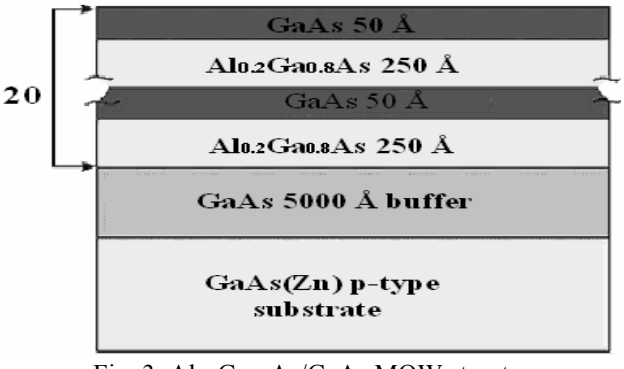


Fig. 3. $Al_{0,2}Ga_{0,8}As$/GaAs MQW structure

3. CHARACTERIZATION OF THE GROWTH $Al_xGa_{1-x}As/GaAs$ STRUCTURES

3.1 X-Ray Characterization

The structure of the growth materials was analyzed by Buker - AXS D8 Discover X-Ray device. (Setup information: Ge 0022 symmetric 4 crystal monochromator (for Si 002 max. FWHM width 0.0035°), KFLCu2K X-Ray source, NaI detector, 1mm detector slit). The obtained X-Ray diffraction pattern was simulated with LEPTOS 1.07 software. The values as layer thicknesses and Al concentration that was appointed by X-ray analysis was suitable with the expected the values of the structure parameters. The graph of I vs 2θ for MQW structure was given in Fig.4 and 5.

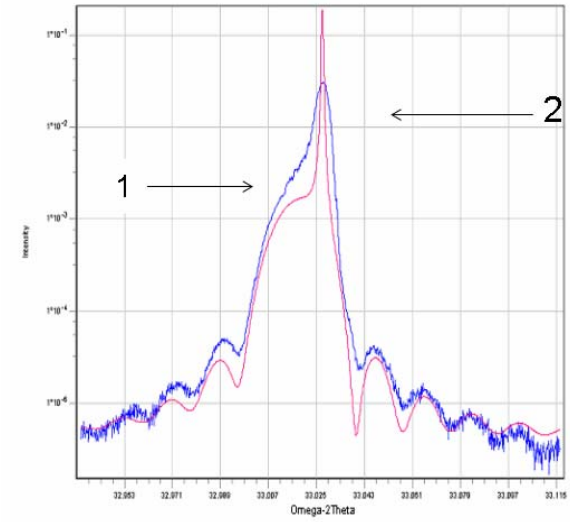


Fig.4. I vs 2θ for $Al_{0,24}Ga_{0,76}As/GaAs$ p-i-n diode (The rocking curve of the structure about GaAs(004) reflection: (1) scan values (experi-menttal) and (2) simulation (computational))

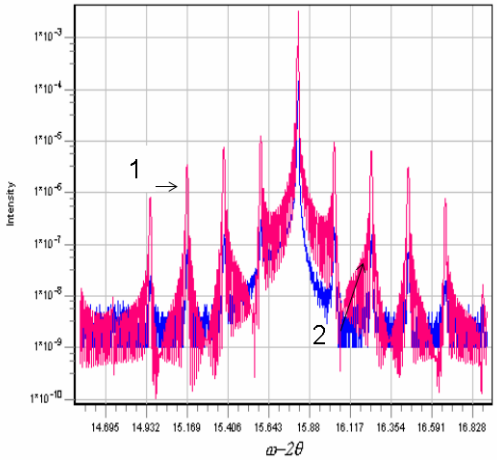


Fig.5. I vs 2θ for $Al_{0,2}Ga_{0,8}As/GaAs$ MQW diode (The rocking curve of the structure about GaAs(002) reflection: (1) scan values (ex-pe-rimental) and (2) simulation (computational))

3.2 Electrical Characterization

The most common theory of a Schottky barrier diode (SBD) based on the Thermionic Emission (TE) model and according to this model the current-voltage(I-V) relationship is given by [7,8]

$$I = I_s\left[\exp(qV_d / kT) - 1)\right] \quad (1)$$

where V_d is the voltage across the junction and I_s is the reverse saturation current and given as:

$$I_s = AA^*T^2 \exp(-q\Phi_{BO} / kT) \quad (2)$$

where A is the area of the diode, A^* the effective Richardson constant, ϕ_{BO} the zero bias barrier height (BH), from I_s value and A values ϕ_{B0} can be calculated. However, some difficulties will arise, if the diode has a series resistance R_s which causes the voltage drop across the junction to be less than the V_d between the terminals of the diode. Also, the downward concave curvature region forward bias I-V plots at sufficiently high voltages has been attributed to the presence of interface states N_{ss}, which equilibrate with the semiconductor, apart from the R_s. Moreover, the BH becomes bias-dependent due to the potential change across the interfacial layers as a result of the applied voltage and N_{ss}. Many methods have been presented to extract the parameters of the diode with only R_s from experimental I-V characteristics [13-16]. However, for the case with a diode with a high series resistances Cheung introduced a method which makes it possible the evaluate the R_s, ϕ_B and ideality factor using a plot of the functions,

$$\frac{dV}{d\ln I} = n\frac{kT}{q} + IR_s \quad (3)$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_B \quad (4)$$

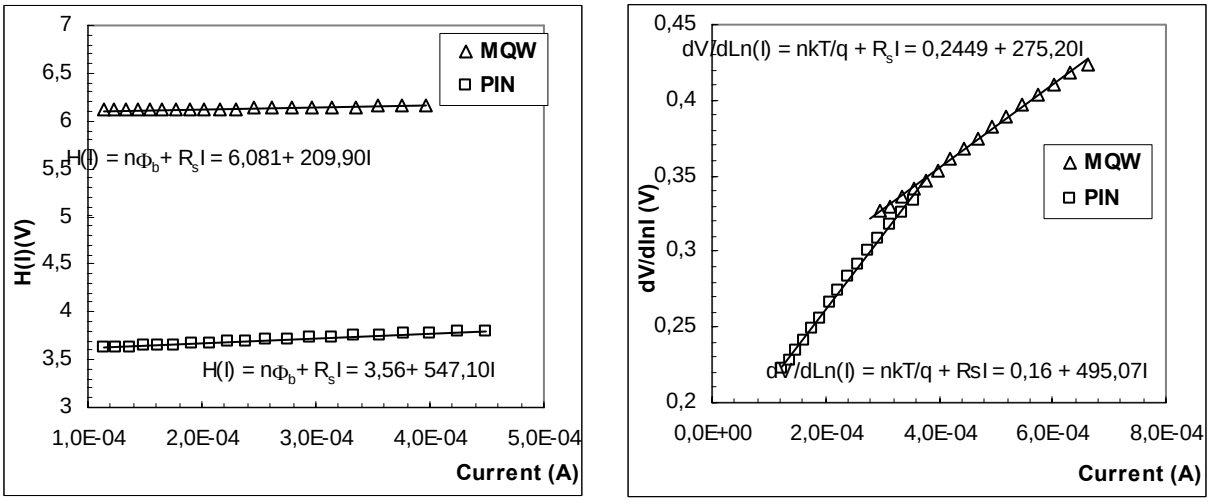
where, Φ_B is the barrier height obtained from data of downward curvature region in the forward bias I-V characteristics. In Figs. 6 (a) and (b), experimental dV/d(lnI) versus I and H(I) versus I plots are presented different temperatures for $Au/Al_{0.24}Ga_{0.76}As/p\text{-}GaAs$ (PIN) and $Au/Al_{0.2}Ga_{0.8}As/p\text{-}GaAs$ (MQW) structures, respectively. Eq. (3) should give straight line for the data of downward bias I-V characteristics. Thus, a plot of dV/d(lnI) versus I will give Rs as the slope and nkT/q as the y-axis intercept. The values of n and Rs derived from Fig.6(a) and are presented in Table 1. Using the n value determined from Eq. (3), and the data of downward curvature region in the forward bias I-V characteristics in Eq.(4) a plot of H(I) versus I according to Eq.(4) will also lead a straight line (as shown in Fig.6(b)) with y-axis intercept equal to $n\Phi_b$. The slope of this plot also provides a second determination of R_s, which can be used to check the consistency of this approach. Thus, by performing different plots (Eqs.(3) and (4)) of the I-V data, three main diode parameters (n, Φ_b and R_s) are obtained and presented in Table1.

Table.1 The obtained n, Io, Φ_{B0} N_{ss}, and R_s values by different techniques for PIN and MQW structures.

Diodes	n (I-V)	I_o (I-V) [A]	Φ_{B0} (I-V) [eV]	N_{ss} [$cm^{-2}eV^{-1}$]	R_s (dV/dlnI) [Ω]	R_s (H(I)) [Ω]
MQW	2,22	$1x10^{-8}$	0,68	$2,09*10^{12}$	275,20	209,90
PIN	5,47	$1x10^{-7}$	0,62	$1,44*10^{13}$	495,07	547,10

The effective BH Φ_e is assumed to be bias-dependent due to the interfacial layer and N_{ss} located at the interfacial layer/semiconductor interface and given as

$$\Phi_e = \Phi_{BO} + \beta(V - IR_s) = \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \quad (5)$$



(a) **(b)**

Fig.6. Plot of (a) dV/dln(I) vs I and (b) H(I) vs I for Au/$Al_{0.24}Ga_{0.76}As$/p-GaAs and Au/$Al_{0.20}Ga_{0.80}As$/p-GaAs, respectively.

The effective BH Φ_e is assumed to be bias-dependent due to the interfacial layer and N_{ss} located at the interfacial layer/semiconductor interface and given as

$$\Phi_e = \Phi_{BO} + \beta(V - IR_s) = \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \quad (6)$$

For N_{ss} in equilibrium with the semiconductor ideality factor is given by [11],

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_0}{W_D} + qN_{ss}(V)\right) \quad (7)$$

where ε_i and ε_s are the permittivities of interfacial layer and semiconductor W_D is the width of the space charge region and δ is the thickness of insulater layer. Both W_D and δ calculated from C^{-2}-V characteristics as W_D(MQW)=$5.40x10^{-6}$ cm, W_D(PIN)=$1.76x10^{-6}$ cm and δ(MQW)=$7.01x10^{-7}$ cm, δ(PIN)=$4.73x10^{-7}$ cm respectively. For the p-type semiconductors, the energy of E_{ss} interface states E_{ss} with respect to the top of valance band E_v at the surface of semiconductor is given by [17,18]

$$E_{ss} - E_v = q(\Phi_e - V) \quad (8)$$

Moreover, the n(V) values for each sample were obtained by

$$I = I_0 \exp\left[\frac{q(V - IR_s)}{n(V)}\right] \quad (9)$$

where I_o=$1x10^{-8}$ and $1x10^{-7}$A and R_s=275.20 and 495.07 Ω for the sample MQW and PIN respectively. Thus, the density distribution curves of N_{ss} obtained from the forward bias I-V characteristics, using $\varepsilon_i=3.5\varepsilon_0$, $\varepsilon_s=12.4\varepsilon_0$, ε_0=$8.85x10^{-14}$ F/cm [7] is given in Fig.7.As shown in Fig.7, both sample PIN and MQW, the interface state density distribution curves never almost a U shape.

In Schottky diodes, the depletion layer capacitance can be expressed as [12]:

$$C^{-2} = \frac{2(V + V_{bi})}{q\varepsilon A^2 N_a} \quad (10)$$

where A is the area of the diode, V reverse bias voltage, V_{bi} built-in(diffusion) potential zero bias and is determined from the extrapolation of the C^{-2} – V plot to the V axis, ε is the dielectric constant of the p-GaAs, N_a is the acceptor concentration of p-type semiconductor. The value of the barrier height can be obtained by the relation:

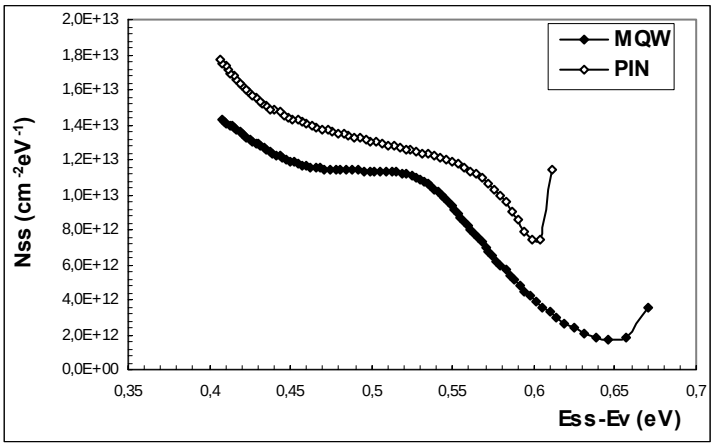
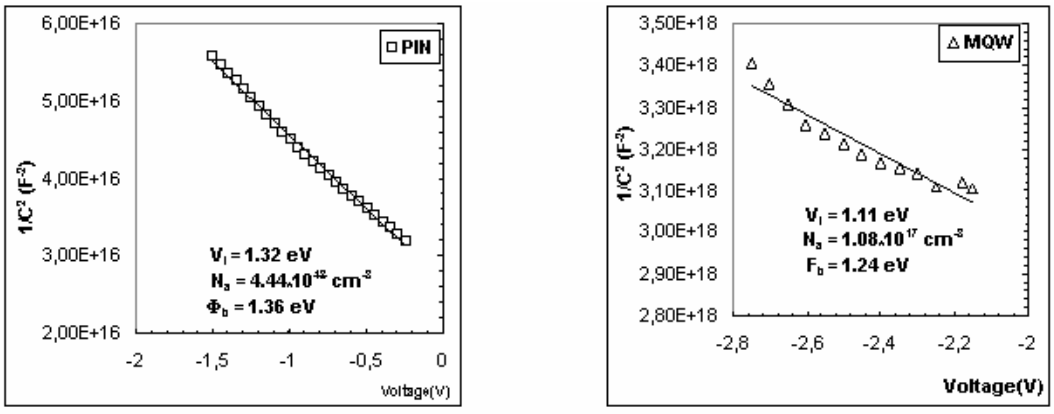


Fig. 7. Density of interface states N_{ss} as a function of E_{ss}-E_v deduced from the forward bias I-V characteristics at room temperature

$$\Phi_{B0}(C-V) = V_{bi} + \frac{kT}{q} + E_F \tag{11}$$

where E_F is the potential difference between the Fermi level and the top of the valance band(E_F-E_v) in the neutral region of p-GaAs can be calculated knowing the carrier concentration:

$$E_F = \frac{kT}{q}\ln\left(\frac{N_a}{N_v}\right) \tag{12}$$



(a) (b)

Fig. 8.Reverse bias $1/C^2$–V characteristics of the a) $Au/Al_{0,24}Ga_{0,76}As/p$-GaAs and b) $Au/Al_{0.2}Ga_{0.8}As/p$-GaAs, respectively.

The reverse C^{-2}–V characteristics(100 kHz) are shown in Fig.8(a) and (b). The linear behavior of the curves can be explained by the fact that the Nss and the inversion layer charge cannot follow the ac signal(100 kHz) and consequently do not contribute appreciably to the diode capacitance. The ϕ_{B0}(C-V) are slightly larger than the ϕ_{B0} (I-V). This difference is explained due to an interface layer or to trap states in the substrate, the effect of the image force and the barrier inhomogeneities.

Acknowledgements: This work is supported by Turkish of Prime Ministry State Planning Organization project number 2001K120590.

4. CONCLUSIONS

The high quality $Al_{0.24}Ga_{0.76}As$/GaAs PIN structure and $Al_{0.2}Ga_{0.8}As$/GaAs multi quantum well structures were growth in the SEMİCON VG80H model MBE system. The structure of the growth materials was analyzed by Buker - AXS D8 Discover X-Ray device. The obtained X-Ray diffraction patterns were simulated using by LEPTOS 1.07 software. The values as layer thicknesses and Al concentration that was appointed by X-ray analysis was suitable with the expected the values of the structure parameters. The *I-V* characteristics of these structures were performed using a Keithley 220 programmable constant current source and a Keithley 614 electrometer. The *C-V* characteristics were performed at 100 kHz by using HP 4192A LF impedance analyzer (5 Hz-13 MHz). The effect of interface state density Nss and series resistance in diodes have been characterized and analyzed. It is found that values of ideality factor obtained from I-V plot was greater than unity. This higher value of n was attributed to an order of magnitude higher density of Nss in PIN diode than in the MQW diode. The high

values of Nss and Rs lead to an important change in the I-V and C-v characteristics and performance of semiconductor devices. In summary, it is clear that ignoring these Rs and Nss can lead to very signification errors in analysis of electrical characteristics.

[1]. S. A. Laurenco , I.. F. L. Dias, E. Laureto , J. L. Duarte et . al , The European Physical Journal B, 21, 11-17 (2001)

[2]. T. Prutskij , P. Diaz Azencibia , F. Silva Andzade, Cryst. Res. Technol. 36 , 4-5, 395-401 (2001)

[3]. V. M. Ustinov , A. E. Zhukov , Semicond. Sci. Technology , 15, R41, (2001)

[4]. M. N. Meynadier, C. Delalande , G. Bastard and M. Voos , Physical Review B, 31, 8(1985)

[5]. S.Wongmanerod et al:Phys. Stat. sol.(b) 210, 615 (1998)

[6]. A. Y. Cho, Journal of Crystal Growth 201/202, 1-7, (1999)

[7]. S. M. Sze, Physics Semiconductor Devices 2nd Ed., New York, (1981).

[8]. E.H. Rhoderick, R.H. Williams, Metal Semiconductor Contacts. 2nd Ed. Oxford, Clarendon Press, (1988).

[9]. N. Konofaos, I.P. McClean, C.B. Thomas, Phys. Stat. Sol. (a) 161 111-118. (1997)

[10]. Ş. Altındal, S. Karadeniz, N. Tuğluoğlu, A. Tataroğlu, Solid-State Elect. 47 1847- 1854, (2003)

[11]. A. Singh, K.C. Reinhart, W.A. Anderson, J. Appl. Phys. 68(7) 3475-3483. (1990)

[12]. H.C. Card, E.H. Rhoderick, J. Phys. D 4 1589-1601. (1971)

[13]. S.K Cheung. , N.W Cheung. Appl.Phys. Lett 49, 85-87, (1986)

[14]. [H. Norde, J. Appl. Phys. 50(7), 50-54 (1979)

[15]. K. E. Bohlin, J. Appl. Phys 60(3), 1223-1224

[16]. A. Keffous, M. Siad, S. Mamma, Y. Bekkacem et al. Appl. Surf. Sci. 218, 336-342, (2003)

[17]. P. Cova, A. Singh, J. Appl. Phys. 82(10), 5217-5226, (1997).

[18]. Ş. Altındal, A. Tataroğlu, İ. Dökme, Solar Energy Materials and Solar Cells 85, 345-358, (2005).