COMPARATIVE STUDY ON THE ELECTRICAL CHARACTERISTICS OF Au/n-Si AND Au/P3HT/n-Si SCHOTTKY CONTACTS

X. HIDIYEV, A. ASIMOV, A. KERIMOVA

G.M. Abdullayev Institute of Physics of NAS Azerbaijan
33, H. Javid ave., Baku, Azerbaijan, AZ-1143
Corresponding author: E-mail address:Hidiyev@gmail.com

In this work, we have fabricated Au/P3HT/n-Si and Au/n-Si Schottky barrier diodes (SBDs) to investigate the effect of polymer interfacial layer on the electronic parameters. Electronic parameters of these two diodes were calculated from the current-voltage characteristics. It was seen that the ideality factor value of 3.47 calculated for the Au/P3HT/n-Si device was higher than the value of 1.18 of the Au/n-Si Schottky diodes. The high values in the ideality factor are caused possibly by various effects such as inhomogeneities of polymer interfacial layer film thickness and series resistance Rs. The Rs values obtained from Cheung's function are 18.6 and 495 for Au/n-Si and Au/P3HT/n-Si, respectively. Our results show that P3HT conductive polymer can be used in device modification for Schottky barrier diodes or photodiodes.

Keywords: Schottky diodes, conductive polymer, spin coating, poly (3-hexylthiophene)
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1. INTRODUCTION

Conductive polymeric materials have advantage such as a good mechanical flexibility, high hole mobility, stable in the atmosphere and easy fabrication [1–5]. There has been much interest in the conductive polymeric materials in the study area of solar cells, light emitting diodes and thin film transistors. The polymeric interfacial layer in metal/polymer/semiconductor (MPS) structures play an important role in the determination of the electrical parameters of these diodes [6-10]. Among the conducting polymers, P3HT has specific properties such as a good mechanical flexibility, high hole mobility and is stable in the atmosphere. The performance of a MPS structures depends on various factors such as presence of the interface states at the metal/ polymer interfacial layer and barrier height and series resistance (Rs) of MPS diodes. Rs and interfacial polymer layer is very important parameter of MPS structures. The electronic parameters of the diodes such as the ideality factor, the barrier height, the interface state density (N_{ss}), the thickness of the interfacial layer and series resistance (R_s) from current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements.

In this study, we will fabricate the Au/P3HT/n-Si metal/polymer/semiconductor (MPS) device by spin coating method. We investigated the electrical parameters of our Au/P3HT/n-Si Schottky diode using forward-bias current–voltage (I–V) measurements and compared the parameters to those for a conventional Au/n-Si diode.

2. EXPERIMENTAL PROCEDURES

n -type Si semiconductor wafer with (100) orientation and 280 mm thickness was used before making contacts, the wafer was chemically cleaned using the RCA cleaning procedure (i.e. 10 min boil in H_2SO_4+ H_2O_2 followed by a 10 min HCl +H_2O_2 +6H_2O at 60^0 C). It was immersed in diluted 20% HF for 60 s. The wafer was rinsed in de-ionized water of resistivity 18 MΩ cm with ultrasonic cleaning in each step. Finally, the sample was dried by exposing the surfaces to high-purity nitrogen. The ohmic contact with a thickness of ~1500 *Å* was made by evaporating 99.9% purity Au metal on the back surface of the n-Si substrate, then was annealed at 550°C for 3 min in N_2 atmosphere. Front surface of samples were coated with a conducting polymer poly(3-hexylthiophene) (P3HT) (fig. 1) film by spin coating (VTC-100) with 1200 rpm for 60 s. After that rectifier, Schottky contacts were formed on the other faces by evaporating ~2000 Å thick Au. We also fabricated Au/n-Si reference diode without the polymer layer to compare with the electrical parameters of the Au/P3HT/n-Si device. All evaporation processes were carried out in a vacuum coating unit at about $5.1x10^{-6}$ Torr. Thus, Au/P3HT/n-Si/Au sandwich Schottky barrier type diode was fabricated. The I−V measurements were performed using a Keithley 6517A electrometer. All measurements were controlled by a computer via an IEEE–488 standard interface so that the data collecting, processing and plotting could be accomplished automatically.

3. ANALYSIS OF AU/P3HT/N-SI JUNCTION DIODE AT ROOM TEMPERATURE

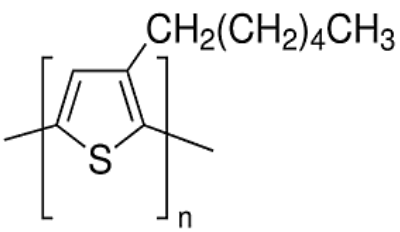

Fig. 1. Molecular structure of P3HT.

The forward-and reverse-bias I–V characteristics of the Au/P3HT/n-Si contact and Au/n-Si diode at room temperature are shown in fig. 2. It is shown that

131, H. Javid ave., AZ-1143, Baku
ANAS, G.M. Abdullayev Institute of Physics
E-mail: jophphysics@gmail.com

the saturation current in these semi-logarithmic plots decreases by P3HT. As clearly seen from fig. 2, the Au/P3HT/n-Si structure exhibits a good rectifying behavior. We analyze the experimental I–V characteristics by the forward bias thermionic emission (TE) theory given as follows [1-2].

$$I=I_0\exp\left(\frac{q\,(V-IR)}{nkT}\right)\left[1-\exp\left(\frac{-q\,(V-IR}{kT}\right)\right] \quad (1)$$

where

$$I_0 = AA^*T\,exp\left(-q\frac{\Phi_{b0}}{kT}\right) \quad (2)$$

is the saturation current, Φ_{b0} (I-V) is the zero bias barrier height, A^* is the Richardson constantant and equals to 120 A cm^{-2} K^{-2} for *n*- type Si, where q is the electron charge, V is the bias voltage, A is the effective diode area, k is the Boltzmann's constant, T is the temperature in Kelvin, n is the ideality factor. From eq. (1), ideality factor n can be written as:

$$n = \frac{q}{kT}\left(\frac{dV}{d(lnI)}\right) \quad (3)$$

n equals to one for an ideal diode. However, n has usually a value greater than unity. High values of n can be attributed to the presence of the interfacial thin native oxide layer and a wide distribution of low-SBH patches (or barrier height inhomogeneities), and, therefore, to the bias voltage dependence of the SBH [1-2]. Φ_{b0} is the zero-bias barrier height (BH), which can be obtained from the following equation

$$\Phi_{b0} = \frac{kT}{q}ln\left(\frac{AA^*T^2}{I_0}\right) \quad (4)$$

Table

The experimental values of some parameters obtained from the forward bias I–V characteristics of Au/n-Si and Au/P3HT/n-Si Schottky barrier diodes at room temperature.

Diodes	n	Φ_b	I_0	dV/dLn(I)		H (I)	
				n	R_s	R_s	Φ_b
Au/n-Si	1,18	0,78	7,56e-9	1,12	18,6	13,5	0,73
Au/P3HT/n-Si	3,47	0,75	2,08E-8	6,07	495	611	0,74

Figure 2 presents the forward bias current–voltage (I–V) characteristics of the Au/P3HT/n-Si/Au structure. The Φ_{b0} and n values of these diodes were calculated from a linear fit of the ln$I$ vs V plots in fig. 2 by using the eqs. (2) and (3) and the obtained values are 0.78 eV and 1.18 for Au/n-Si/Au diode, 0.75 eV and 3,47 for Au/P3HT/n-Si/Au diode, respectively. It has been observed that ideality factor of Au/P3HT/n-Si structure increases about 2.29 with respect to Au/n-Si at room temperature. The value of the ideality factor is greater than unity. The high values in the ideality factor are caused possibly by various effects such as inhomogeneities of P3HT film thickness, non-uniformity of the interfacial charges and series resistance, [11-14]. The values of the series resistance is determined from following functions using eq. (4).

$$\frac{dV}{d(lnI)} = IR_s + n\left(\frac{kT}{q}\right) \quad (5)$$

$$H(I) = V - n\left(\frac{kT}{q}\right)ln\left(\frac{I_0}{AA^*T^2}\right) \quad (6)$$

In fig. 3 (a) and (b), the values of dV/d (ln I)–I and H(I)–I are plotted for Au/P3HT/n-Si and Au/n-Si Schottky contacts, respectively. A plot of dV/dln (I) vs I will gives Rs as the slope and n the y- axis intercept [15, 16]. The values of n and Rs for SBD were derived from fig. 3 by using eqs. (5) and (6), respectively, and they were presented in table 1. The R_s values obtained from eq. (5) are 18.6 and 495 for Au/n-Si and Au/P3HT/n-Si respectively. The high series resistance R_s value can be attributed to the presence of a native interfacial layer between metal and semiconductor.

The interface states and interfacial layer between the metal/semiconductor structures play an important role in the determination of the electronic parameters of the diodes.

Density of interface states proposed by Card and Rhoderick can be simplified and given as [17, 18]:

$$N_{ss}(V) = \frac{1}{q}\left\{\frac{\varepsilon_i}{\delta}[n(V)-1] - \frac{\varepsilon_s}{W_D}\right\} \quad (7)$$

where N_{ss} is the density of the interface states, δ is the thickness of interfacial layer, W_d is the space charge width, and n(V) is the voltage-dependent ideality factor, ε_s=11.8ε_0 and ε_i=3ε_0 are the permittivity of the semiconductor and conducting polymer (P3HT), respectively. In n -type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of the semiconductor is given by

$$E_c - E_{ss} = q(\Phi_e - V_D) \quad (8)$$

where V_D is the applied voltage drop across the depletion layer and Φ_e is the effective barrier height. N_{ss} values are obtained via eq. (7). Figure 4 shows the energy distribution profiles of N_{ss} extracted from the forward bias I–V characteristics for Au/P3HT/n-Si and Au/n-Si Schottky barrier diodes. The magnitude of N_{ss} ranges from 5.05x10^{11} at Ec-0.63 eV to 2.01x10^{12} eV^{-1} cm^{-2} at Ec-0.46 eV for Au/P3HT/n-SiSBD and 5.46x10^{11} at Ec-0.61 eV to 6.33x10^{11} eV^{-1} cm^{-2} at Ec-0.47 eV for Au/n-Si Schottky barrier diodes.

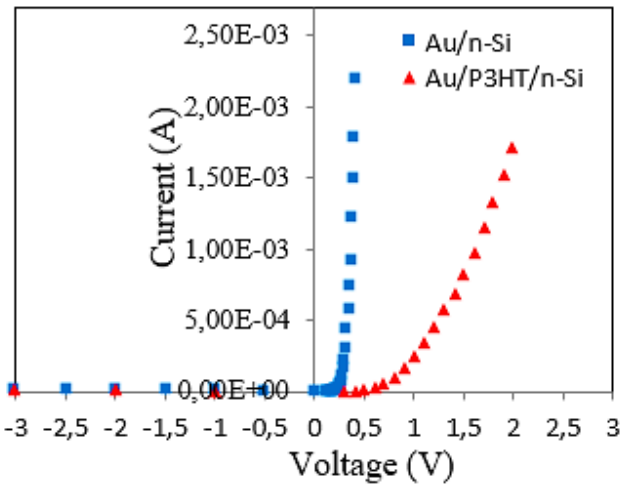

Fig. 2. The forward and reverse bias semi-logarithmic I–V characteristics of Au/n-Si and Au/P3HT/n-Si Schottky barrier diodes at room temperature.

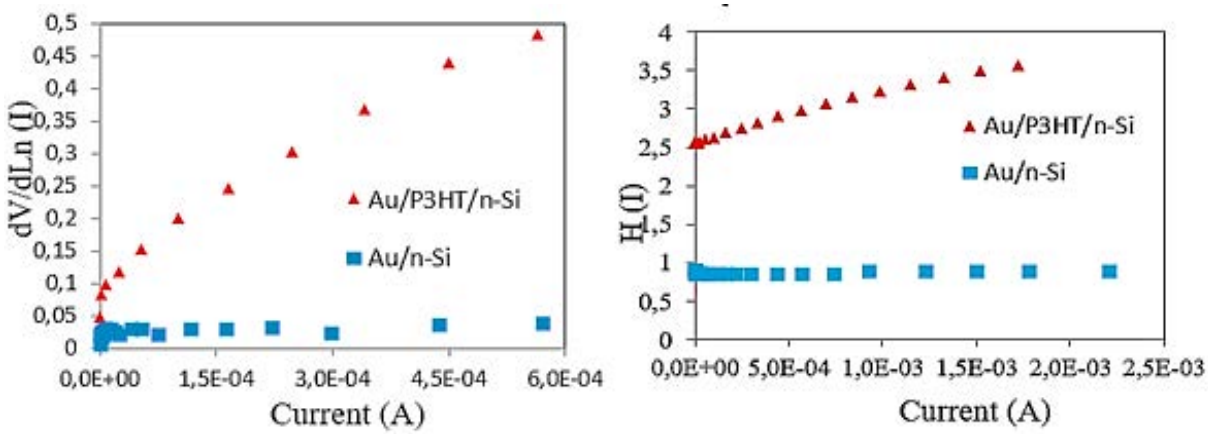

Fig 3. The plots of dV/d ln I and H (I) vs. current of Au/n-Si and Au/P3HT/n-Si Schottky barrier diodes at room temperature.

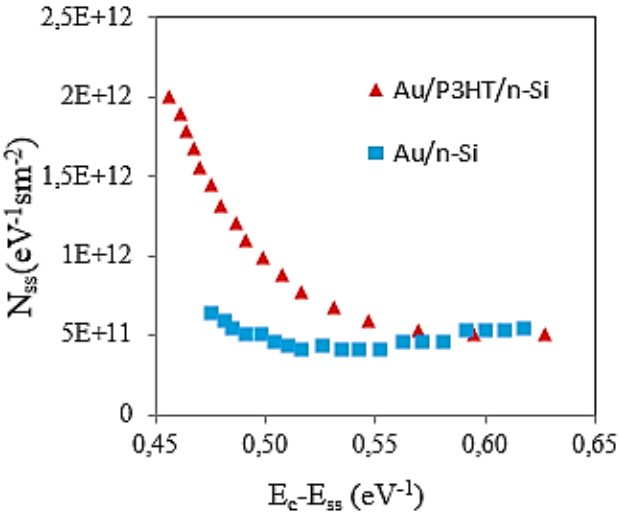

Fig. 4. The energy distribution profiles of N_{ss} for Au/n-Si and Au/P3HT/n-Si Schottky barrier diodes at room temperature.

4. CONCLUSION

Electronic properties of the Au/n-Si and Au/P3HT/n-Si Schottky barrier diode have been investigated by means of I–V measurements at room temperature. It was seen that the ideality factor value of 3.47 eV calculated for the Au/P3HT/n-Si device was higher than the value of 1.18 eV of the Au/n-Si Schottky barrier diodes. The values of the ideality factor, series resistance and barrier height obtained from Cheung and Norde method were compared, and it was seen that there was an agreement with each other.

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